


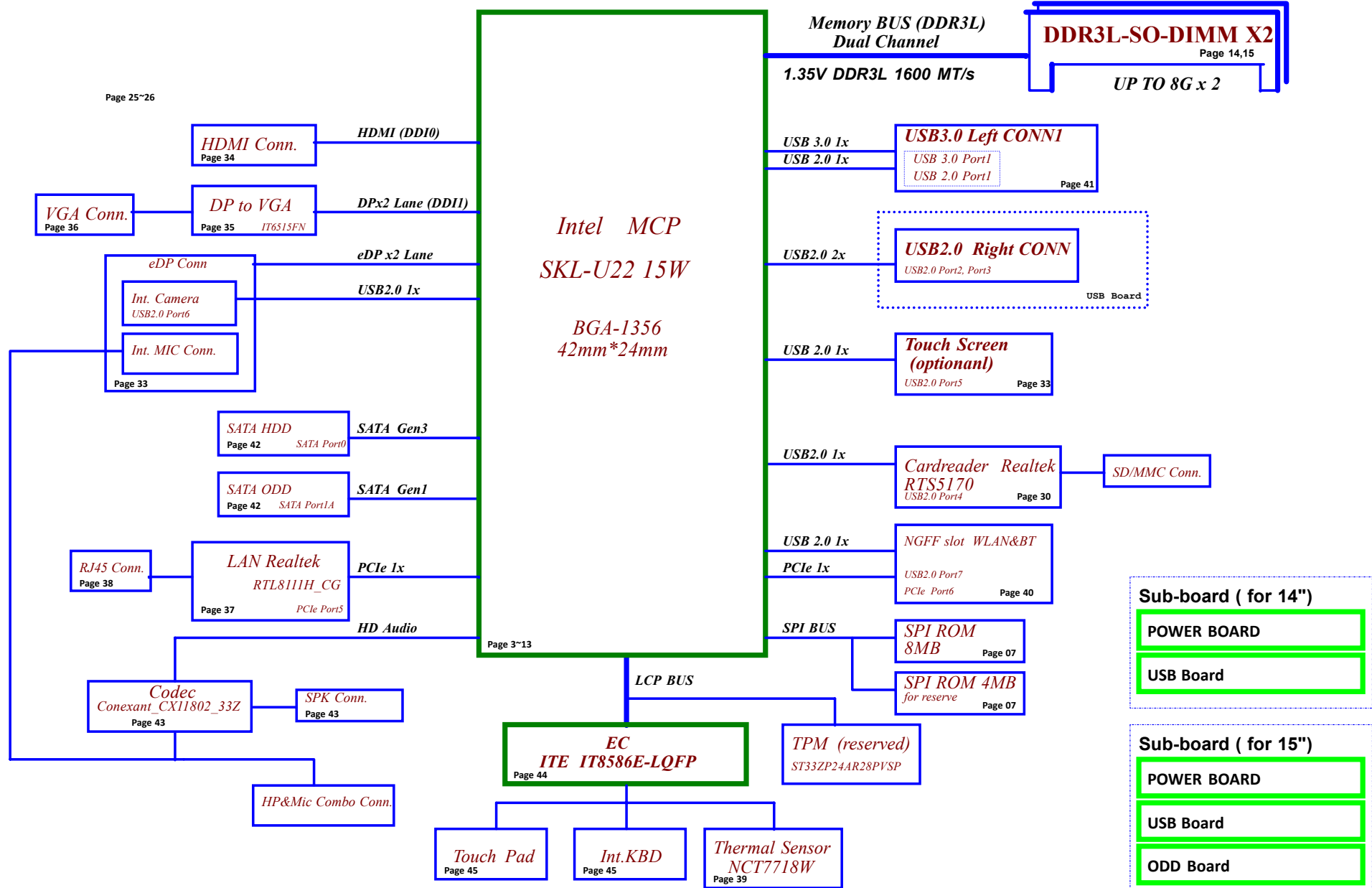
BMWQ1/Q2 UMA M/B Schematics Document

Intel Skylake U22 with DDRIIL

2015-07-12

REV:1.0

Security Classification		LC Future Center Secret Data		Title					
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Voltage Rails (0 --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.35V +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.675VS
S0	0	0	0	0
S3	0	0	0	X
S3 Battery only	0	0	0	X
S5 S4/AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function	BOM Structure	BTO Item
USB3.0	1 USB3.0 CONN left	@	Not stuff
	2 NC	14@	For 14" part
	3 NC	15@	For 15" part
	4 NC	14or15@	For 14" or 15" part
	5 NC	14or17@	For 14" or 17" part
	6 NC	AOAC@	AOAC support part
USB2.0	1 USB3.0 CONN Left	BCD@	For C cost down (BDW)
	2 USB2.0 CONN1 Right	Cannonlake@	For Cannonlake part
	3 USB2.0 CONN2 Right	CD@	For C cost down
	4 Camera	DUALMIC@	For Dual MIC part
	5 Cardreader	EMC@	For EMC part
	6 Touch Panel	EMC_15@	For EMC 15" part
	7 BT	EMC_NS@	For EMC nu-stuff part
	8 NC	EMC_PX@	For EMC PX part
	9 NC	EMC_PXNS@	For EMC PX nu-stuff part
	10 NC	ES@	For ES CPU
PCIE	1 NC	EXO@	For EXO GPU
	2 NC	GCLK@	For GreenCLK part
	3 NC	ME@	For ME part
	4 NC	NTS@	For nu-touch part
	5 LAN	PCH_SDIO@	For PCH SDIO part
	6 WLAN	PCH_SDIO1@	For PCH SDIO path1
	7 used as SATA	PCH_SDIO2@	For PCH SDIO path2
	8 used as SATA	PX@	For PX part
SATA	X4 PCIE (9-12)	RANKA@	For VRAM rank A part
		RANKB@	For VRAM rank B part
		Realtek SD@	For Realtek SD part
		SINGLEMIC@	For single MIC part
		SINGLERANK@	For single VRAM rank part
		DUALRANK@	For dual VRAM rank part
		TS@	For touch screen part
		TPM@	For TPM part
		UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charge	DGPU
EC_SMB_CK1	IT8586E	V	V	X	X	X	X	X	V	X
EC_SMB_DA1	+3VALW	V	+3VALW	X	X	X	X	X	V	X
EC_SMB_CK2	IT8586E	X	V	X	X	V	V	X	X	V
EC_SMB_DA2	+3VS	X	+3VS	X	X	+3VS	+3VALW_PCH	X	X	+3VGS
PCH_SMB_CLK	PCH	X	X	V	V	X	V	X	X	X
PCH_SMB_DATA	+3VALW_PCH	X	X	+3VS	+3VS	X	+3VALW_PCH	X	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

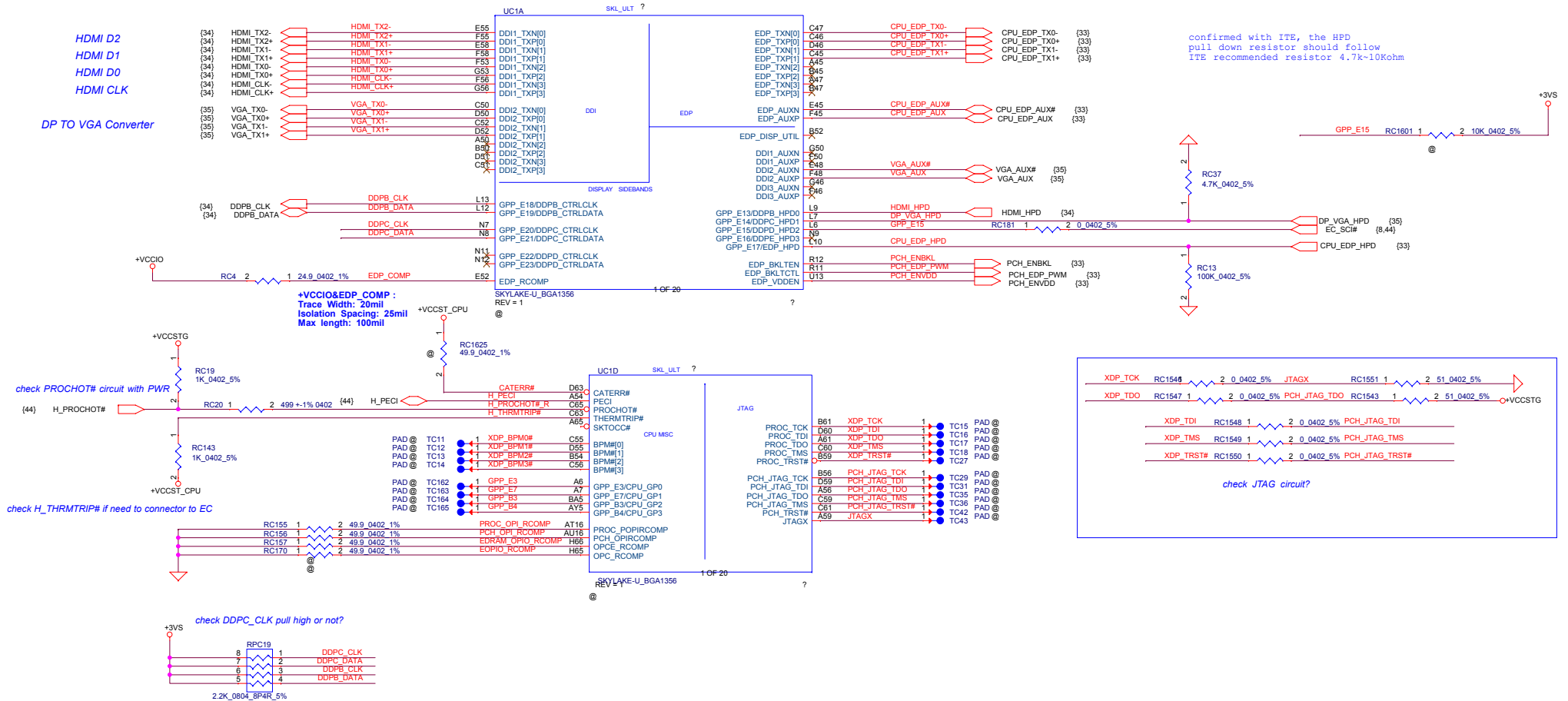
EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	1001_100xb
PCH	need to update
DGPU	need to update

PCH SM Bus address

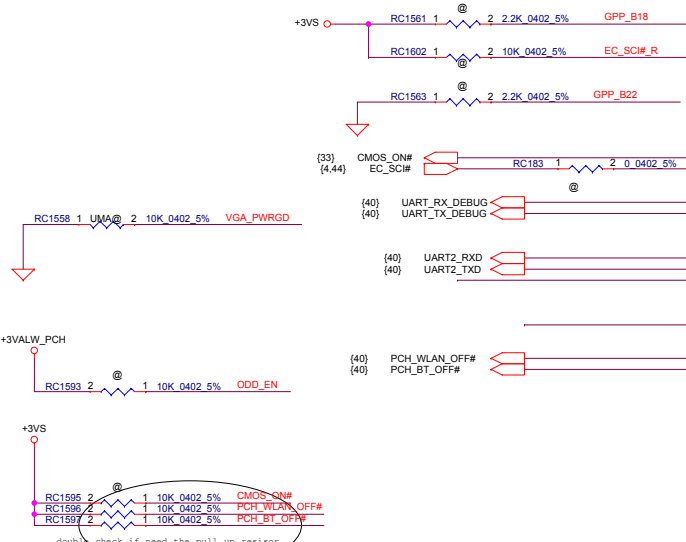
Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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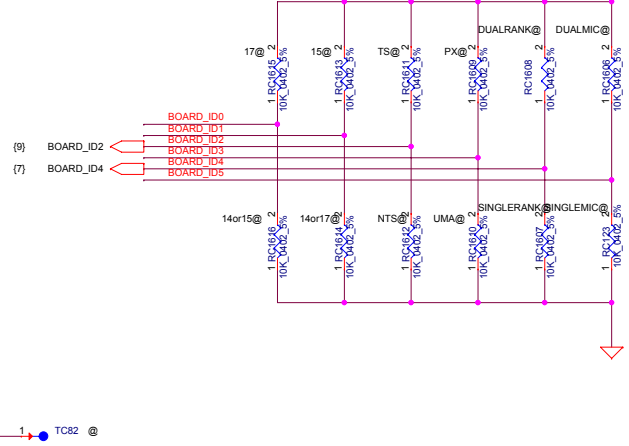
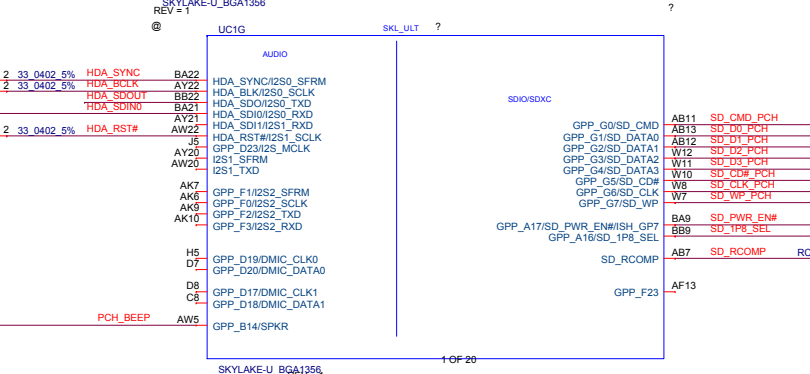
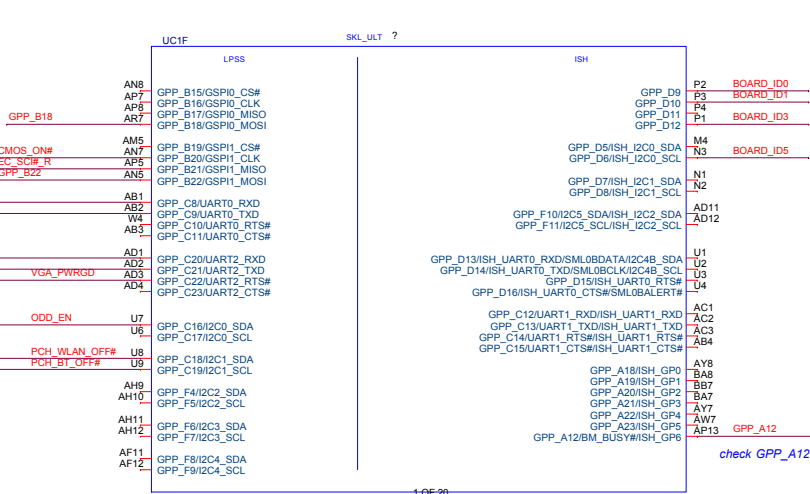
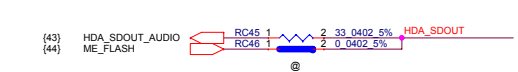
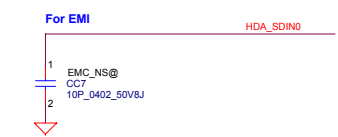


DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC



HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



Board ID	Description	Stuff R
Board_ID[0:1]	00	14"
	01	15"
	10	17"
	11	Reserved
Board_ID2	0	Non-touch
	1	Touch
Board_ID3	0	SingleRank
	1	DualRank
Board_ID4	0	SingleMIC
	1	DualMIC

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GPIO0 MOSI/No Reboot /GPP_B18		Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GPIO1 MOSI/Boot BIOS /GPP_B22	Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

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Title

MCP (LPSS,ISH,AUDIO,SD)

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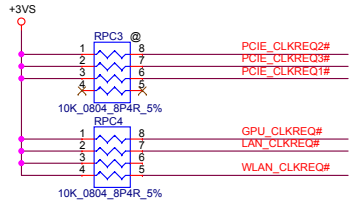
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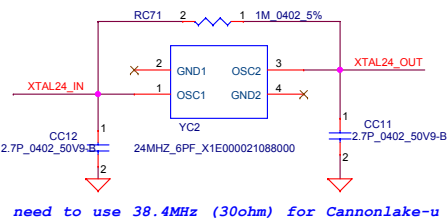
check the Pull up resistor



PCIE CLK5 LAN

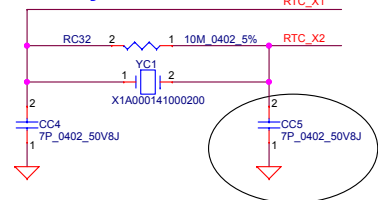
PCIE CLK6 WLAN

check if need to change to 1M_0402_1% follow PDG, CRB is 1M_0402_5%

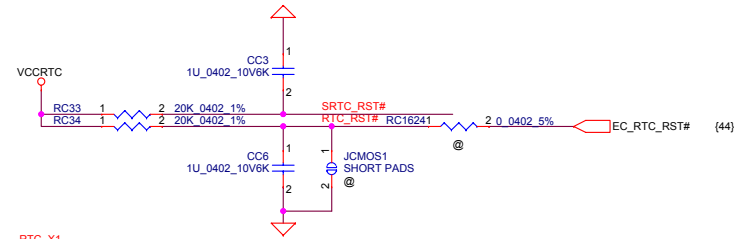
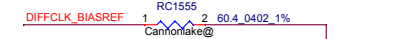
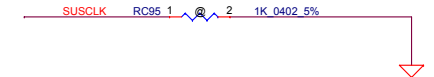
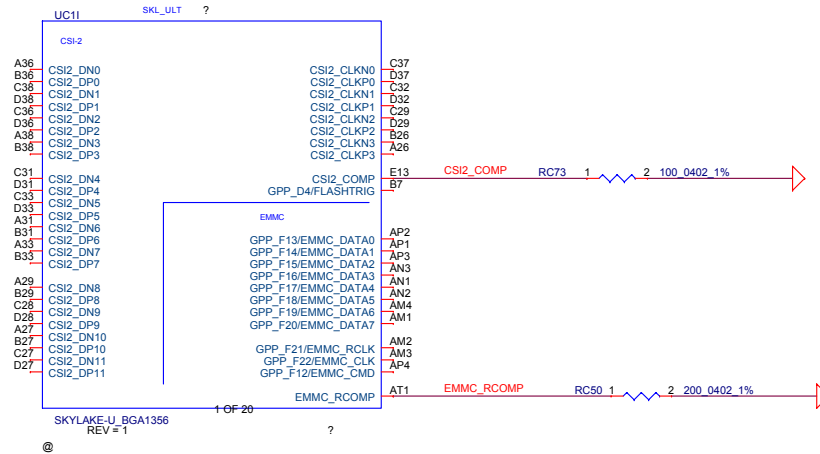


(31) 24M_CLK RC122 1 2 0.0402 5% XTAL24_IN

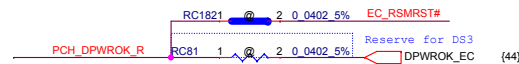
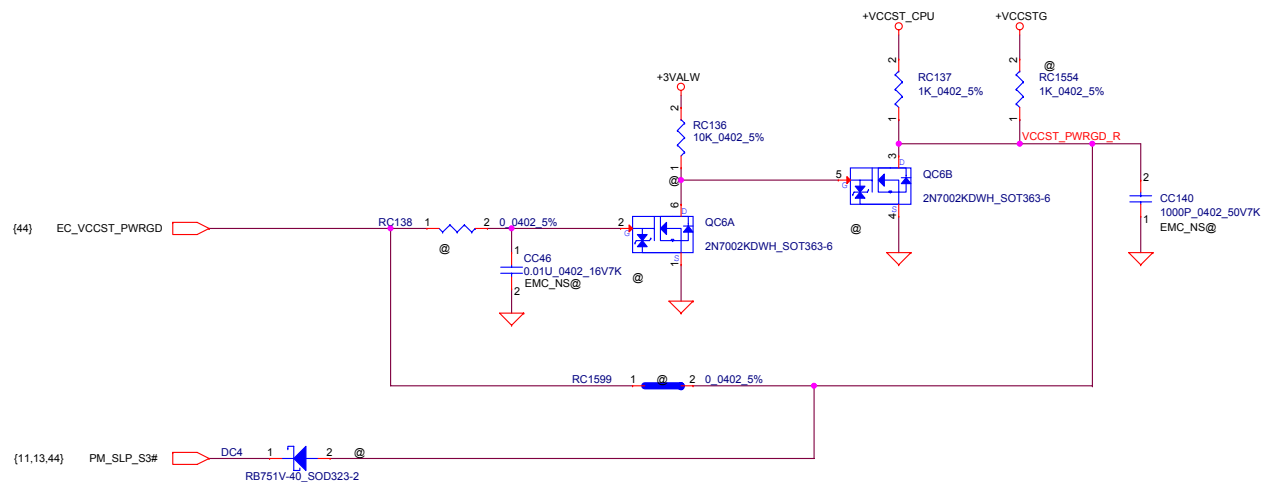
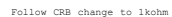
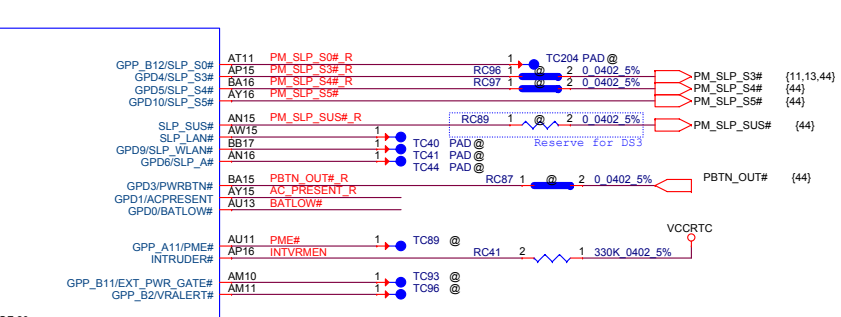
change to SJ10000LM00



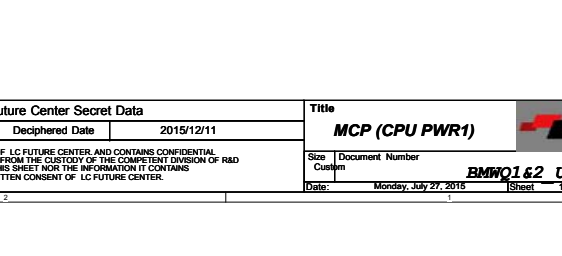
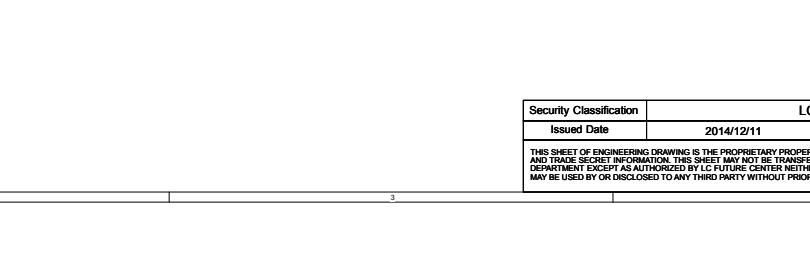
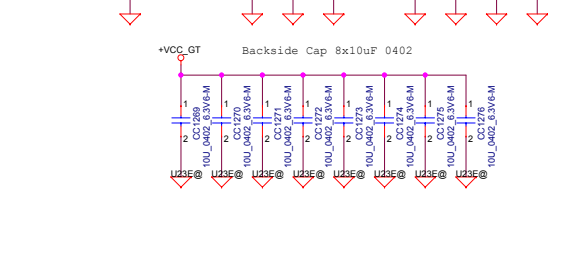
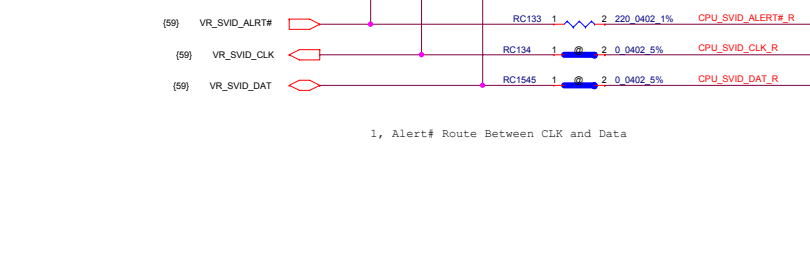
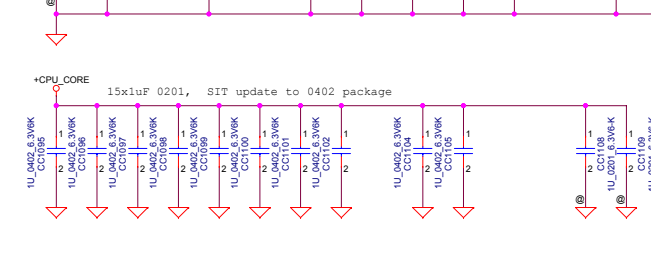
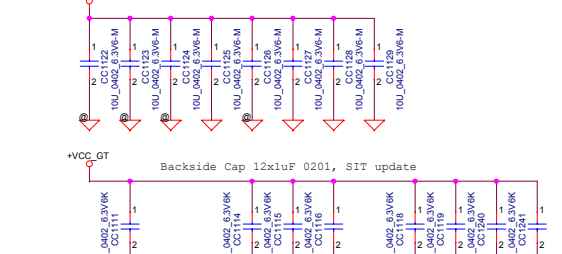
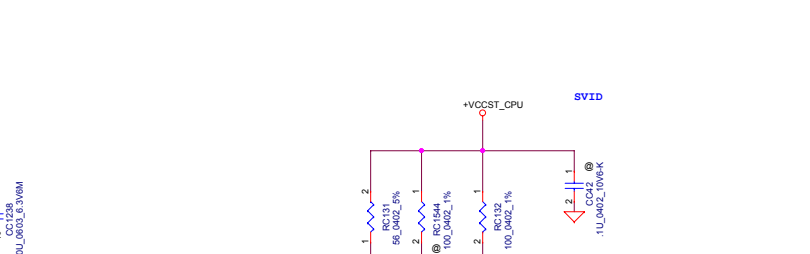
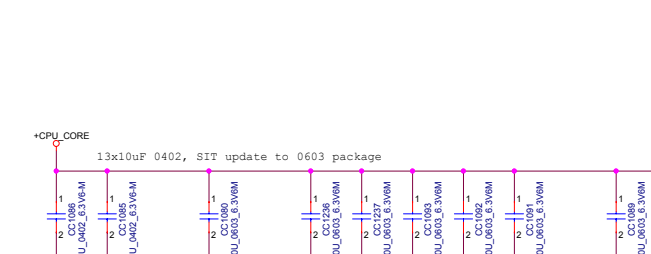
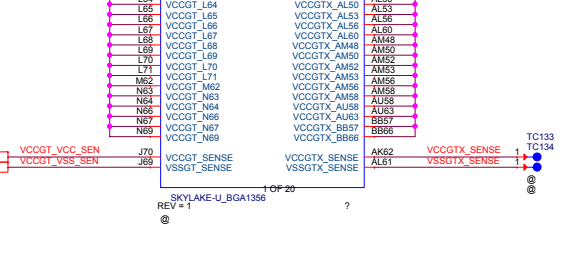
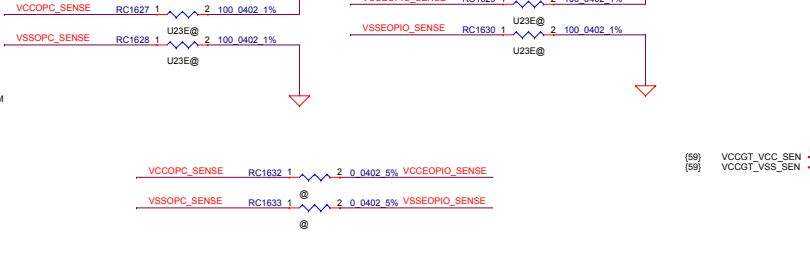
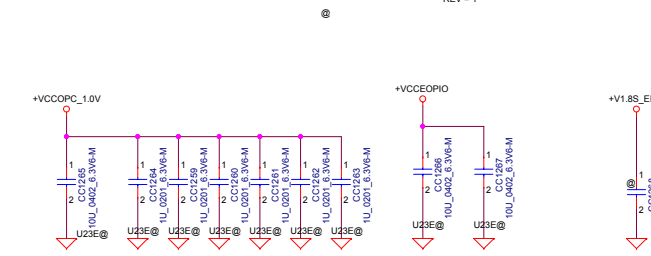
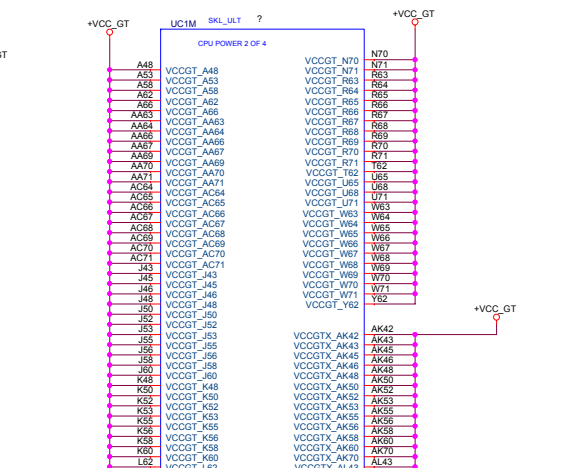
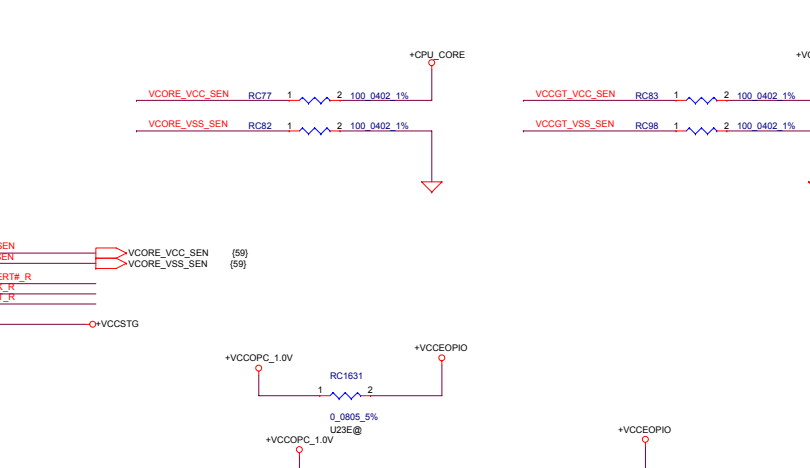
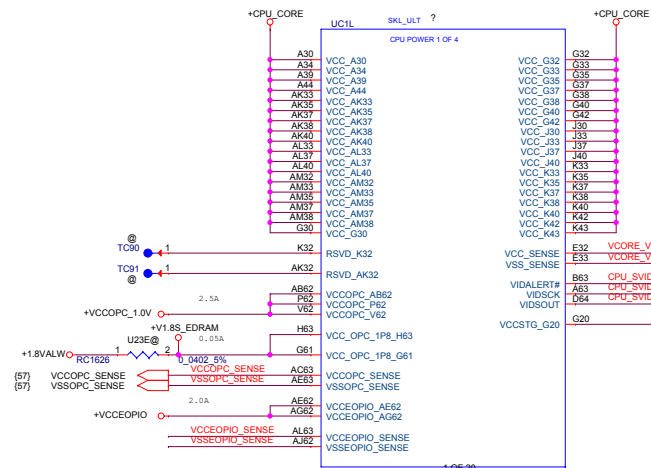
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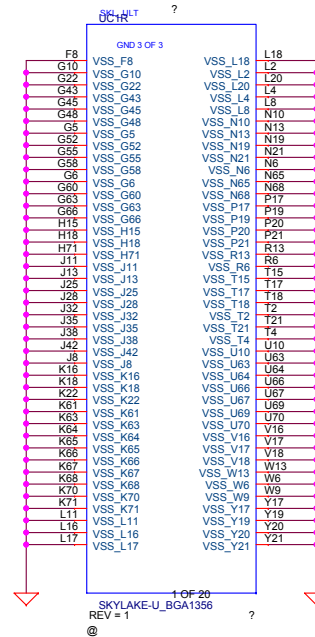
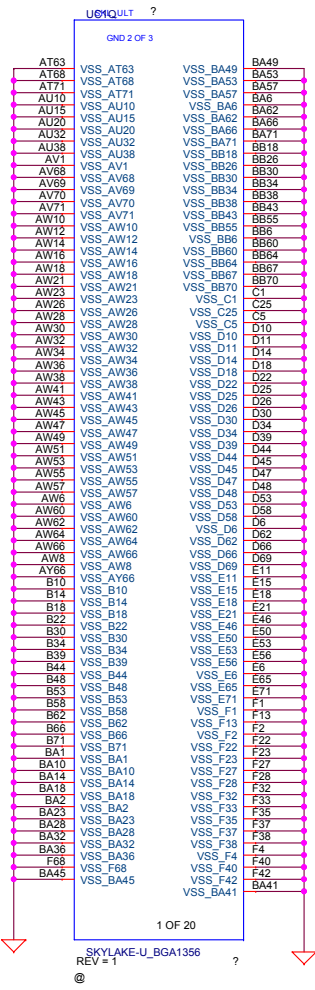
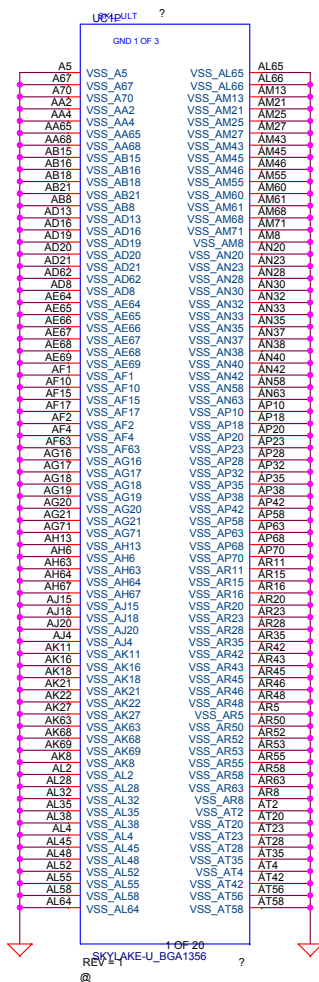


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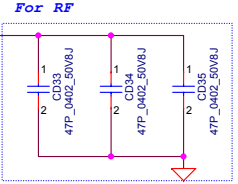
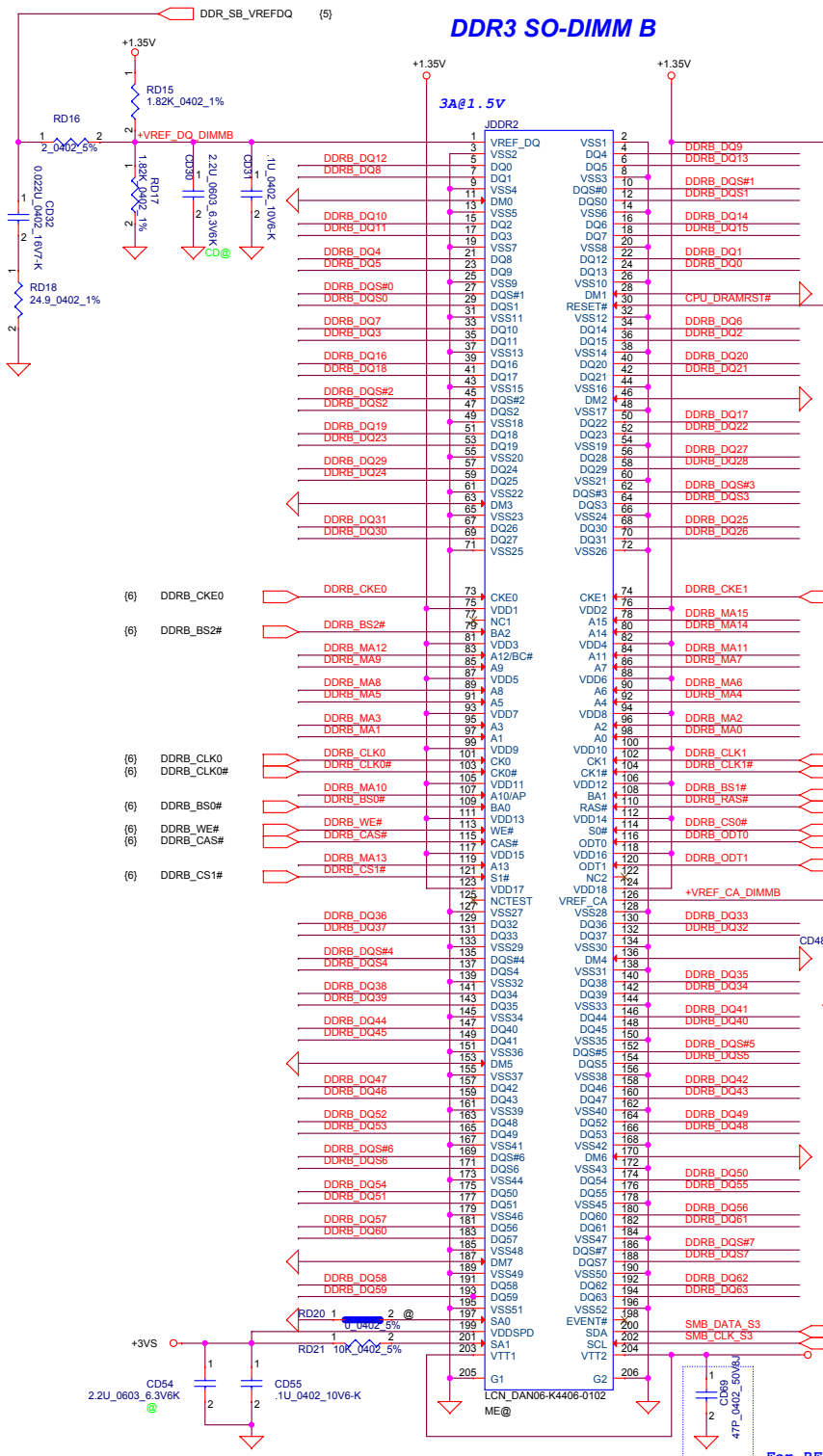




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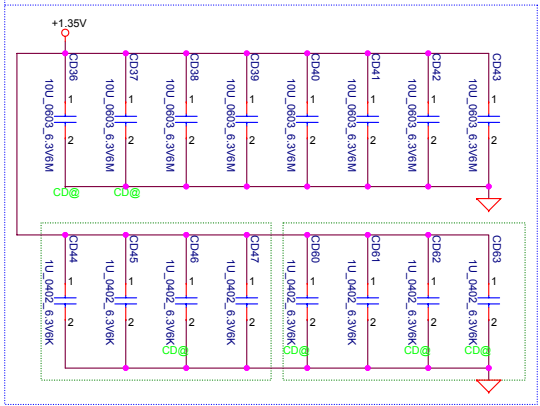
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DDR SO-DIMM B



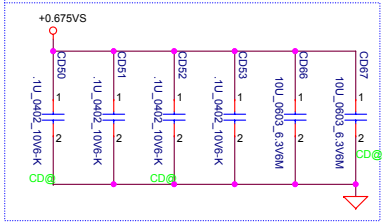
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Place near DIMM

(10uF_0603_6.3V)*8
(1u_0402_6.3V)*8



Layout Note:
Place near DIMM

(100_0603_6.3V)*2
(.1u_0402_10V)*4



Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDR_B_DQ12
7	DQ1	DDR_B_DQ8
15	DQ2	DDR_B_DQ10
17	DQ3	DDR_B_DQ11
4	DQ4	DDR_B_DQ9
6	DQ5	DDR_B_DQ13
16	DQ6	DDR_B_DQ14
18	DQ7	DDR_B_DQ15
10	DQS#0	DDR_B_DQS#1
12	DQS0	DDR_B_DQS1
21	DQ8	DDR_B_DQ4
23	DQ9	DDR_B_DQ5
33	DQ10	DDR_B_DQ7
35	DQ11	DDR_B_DQ3
22	DQ12	DDR_B_DQ1
24	DQ13	DDR_B_DQ0
34	DQ14	DDR_B_DQ6
36	DQ15	DDR_B_DQ2
27	DQS#1	DDR_B_DQS#0
29	DQS1	DDR_B_DQS0
39	DQ16	DDR_B_DQ16
41	DQ17	DDR_B_DQ18
51	DQ18	DDR_B_DQ19
53	DQ19	DDR_B_DQ23
40	DQ20	DDR_B_DQ20
42	DQ21	DDR_B_DQ21
50	DQ22	DDR_B_DQ17
52	DQ23	DDR_B_DQ22
45	DQS#2	DDR_B_DQS#2
47	DQS2	DDR_B_DQS2
57	DQ24	DDR_B_DQ29
59	DQ25	DDR_B_DQ24
67	DQ26	DDR_B_DQ31
69	DQ27	DDR_B_DQ30
56	DQ28	DDR_B_DQ27
58	DQ29	DDR_B_DQ28
60	DQ30	DDR_B_DQ25
70	DQ31	DDR_B_DQ26
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129	DQ32	DDR_B_DQ36
131	DQ33	DDR_B_DQ37
141	DQ34	DDR_B_DQ38
143	DQ35	DDR_B_DQ39
130	DQ36	DDR_B_DQ33
132	DQ37	DDR_B_DQ32
140	DQ38	DDR_B_DQ35
142	DQ39	DDR_B_DQ34
135	DQS#4	DDR_B_DQS#4
137	DQS4	DDR_B_DQS4
147	DQ40	DDR_B_DQ44
149	DQ41	DDR_B_DQ45
157	DQ42	DDR_B_DQ47
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148	DQ45	DDR_B_DQ40
158	DQ46	DDR_B_DQ42
160	DQ47	DDR_B_DQ43
152	DQS#5	DDR_B_DQS#5
154	DQS5	DDR_B_DQS5
163	DQ48	DDR_B_DQ52
165	DQ49	DDR_B_DQ53
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166	DQ53	DDR_B_DQ48
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176	DQ55	DDR_B_DQ55
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191	DQ58	DDR_B_DQ58
193	DQ59	DDR_B_DQ59
180	DQ60	DDR_B_DQ56
182	DQ61	DDR_B_DQ61
192	DQ62	DDR_B_DQ62
194	DQ63	DDR_B_DQ63
186	DQS#7	DDR_B_DQS#7
188	DQS7	DDR_B_DQS7

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Date

DDR III SO-DIMM B

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Monday, July 27, 2015

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Sheet

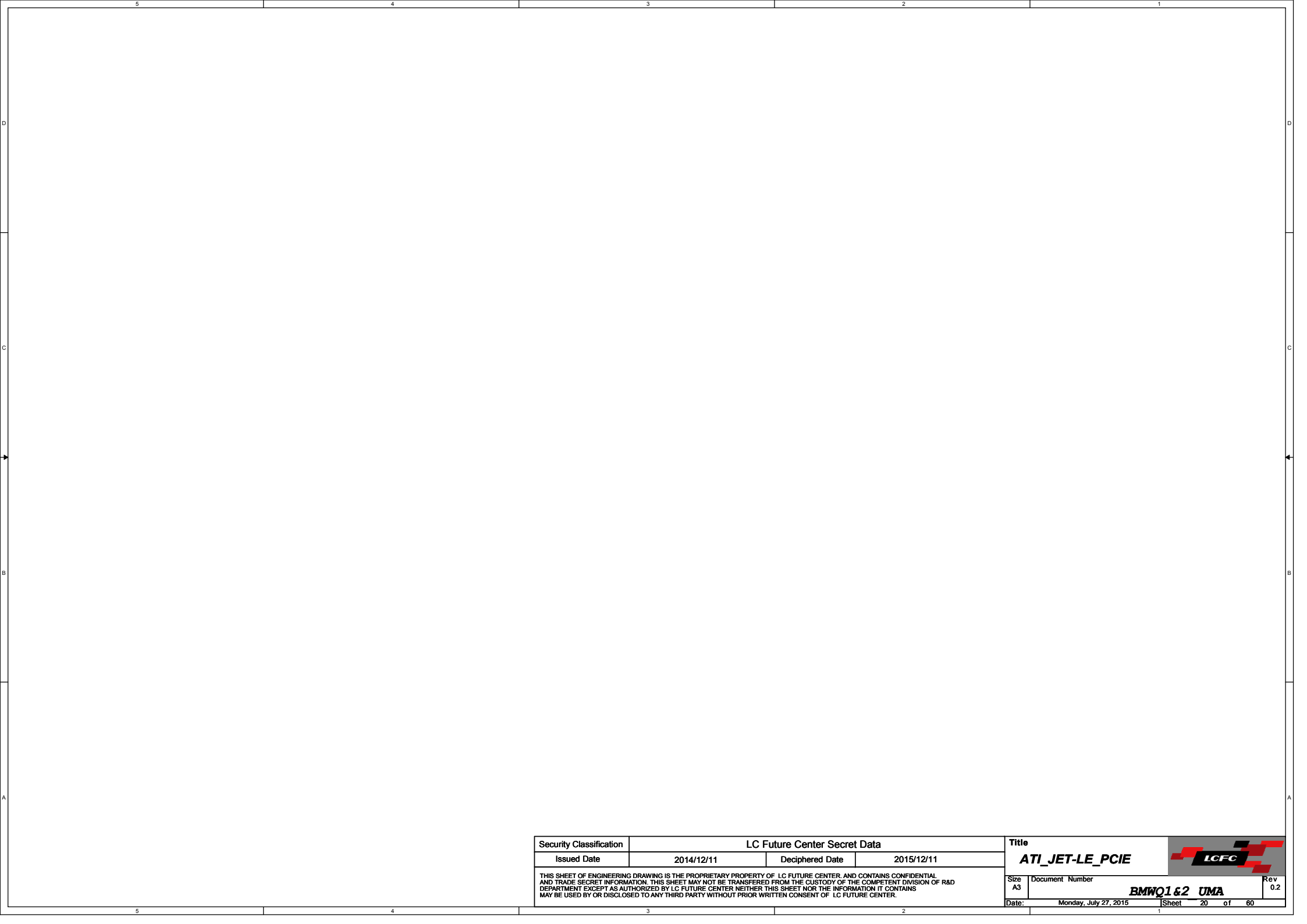
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C				C																																
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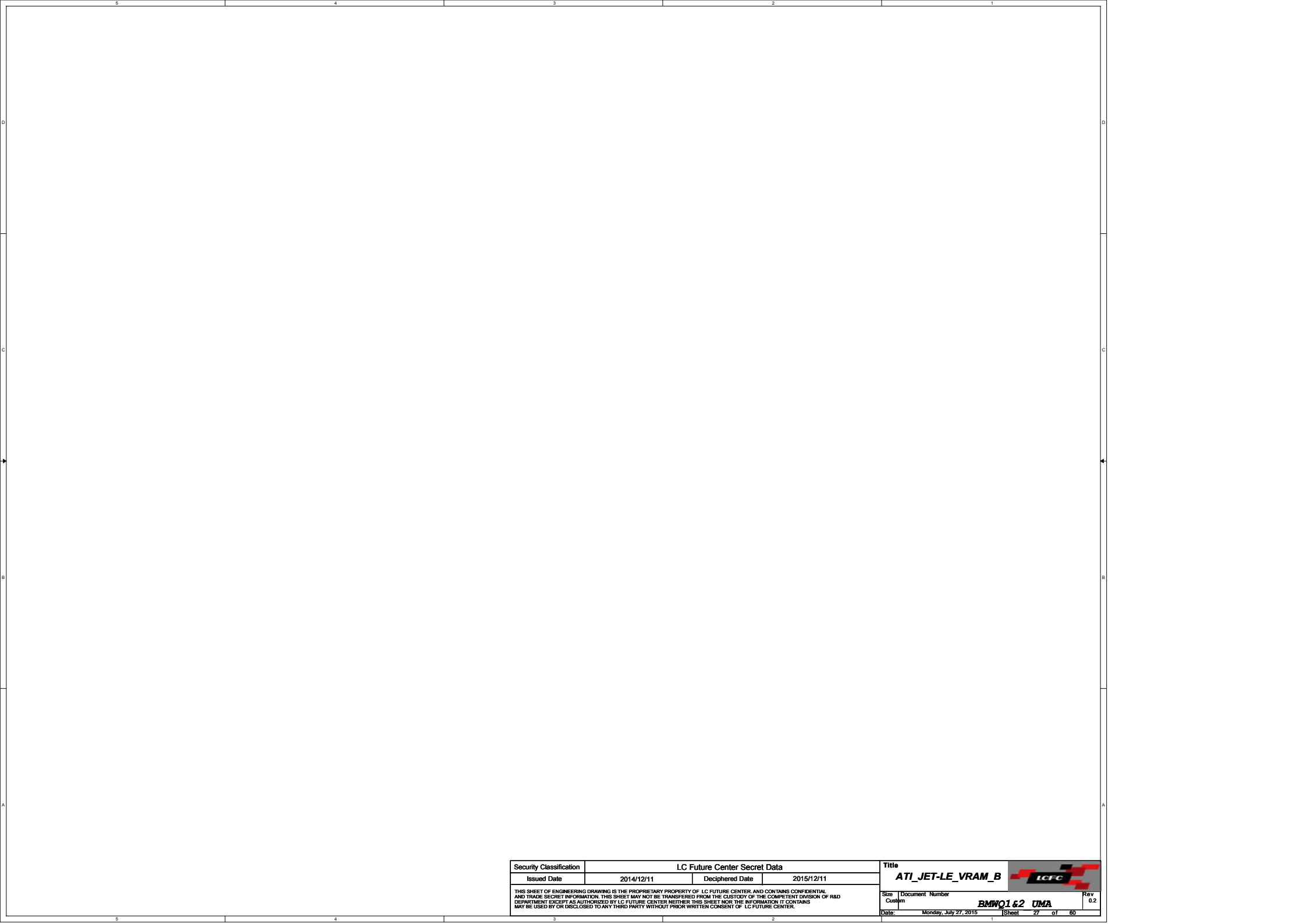
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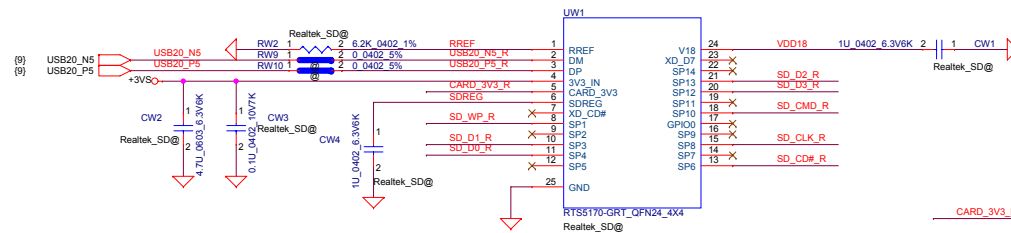
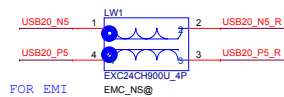


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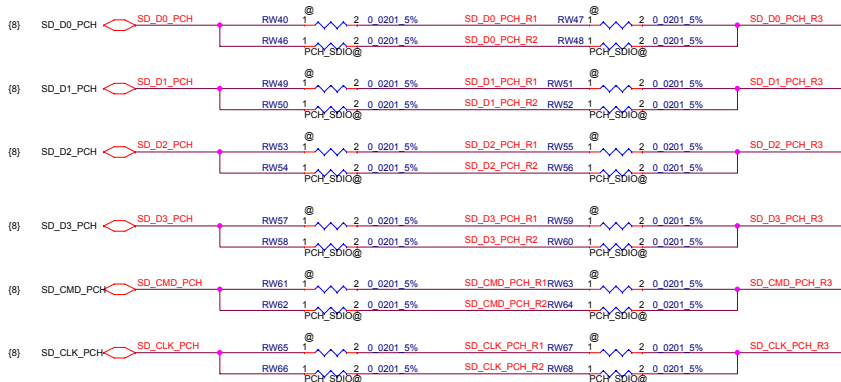
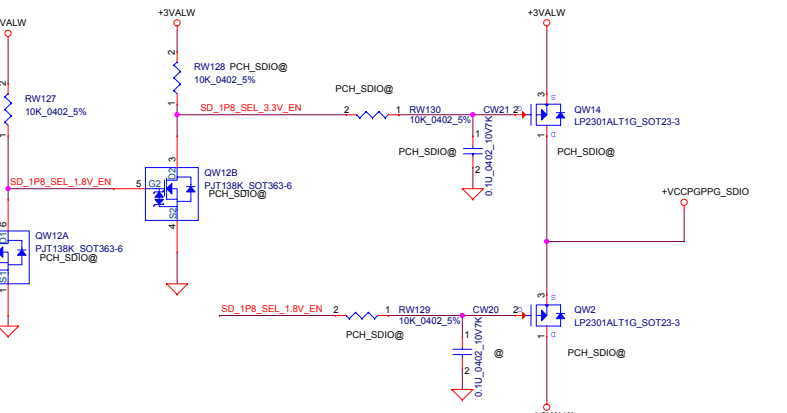
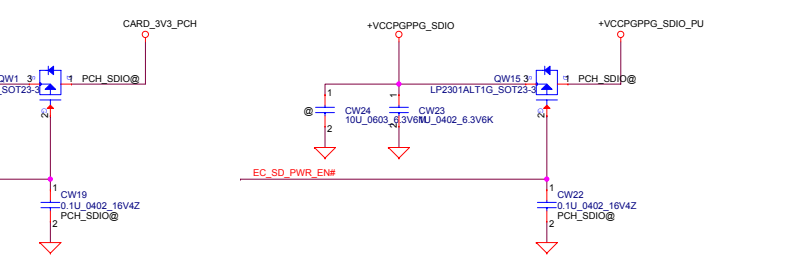
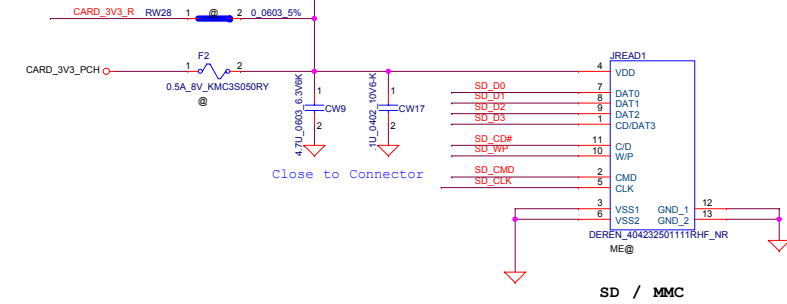
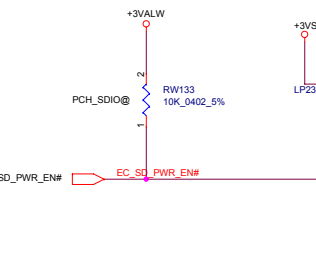
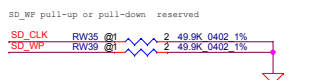
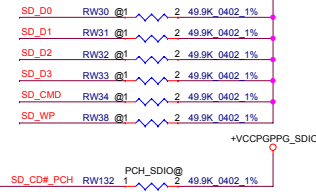
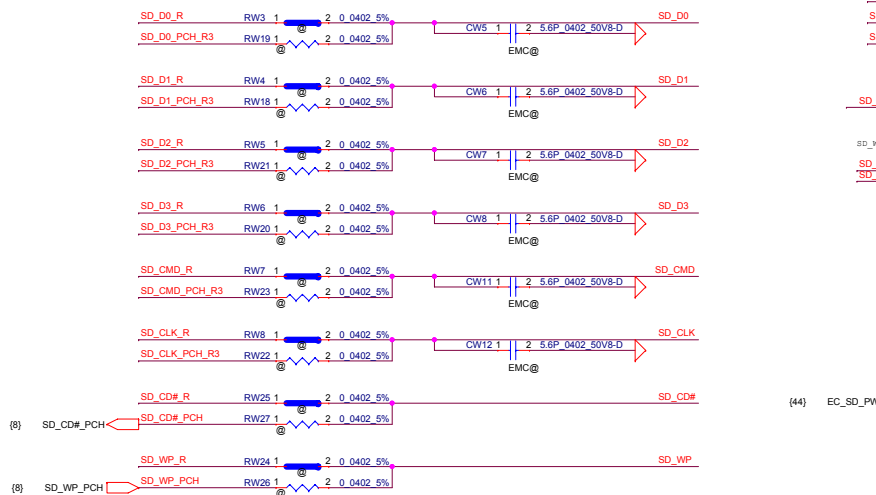
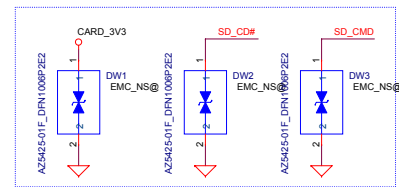
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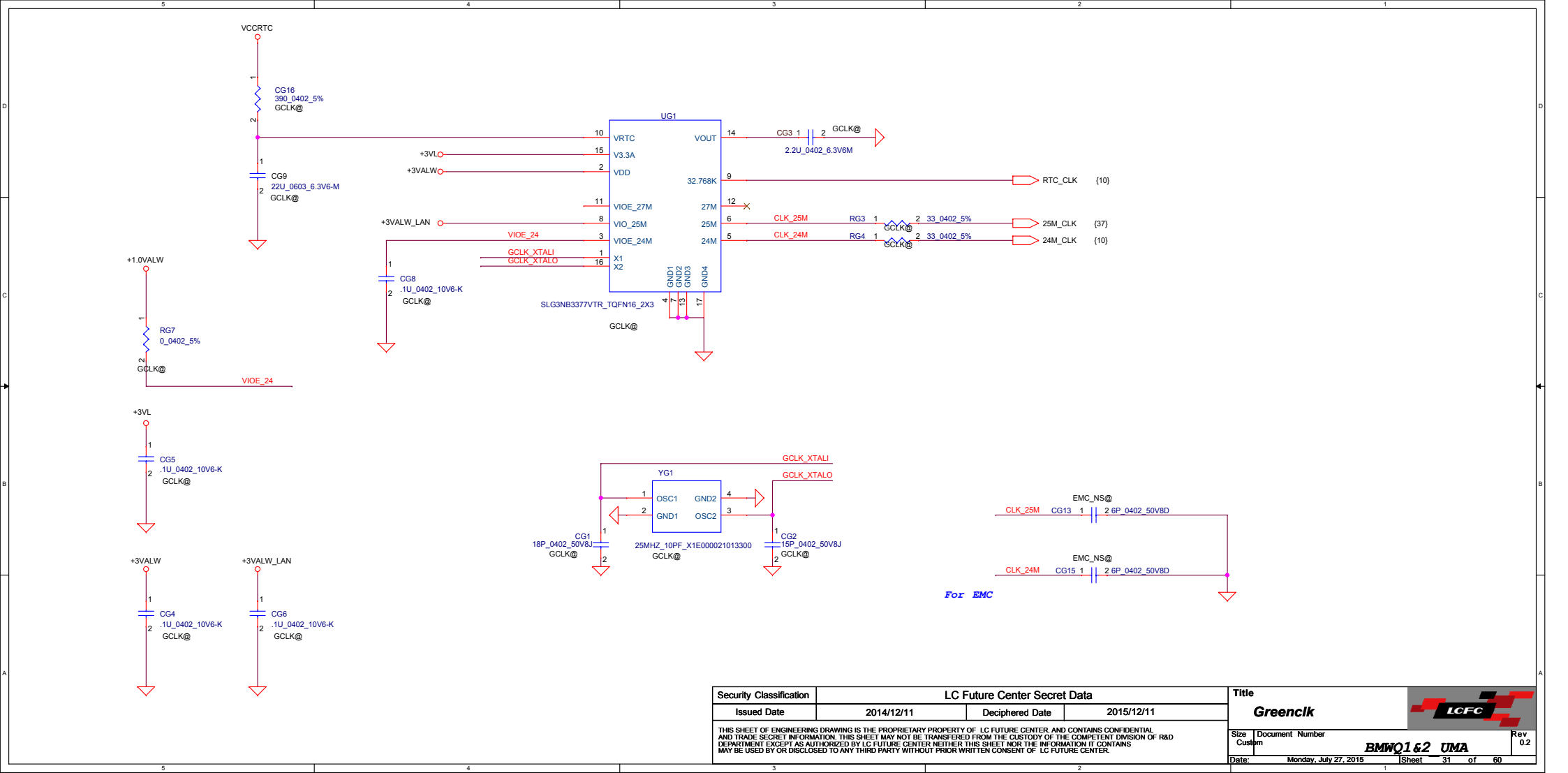


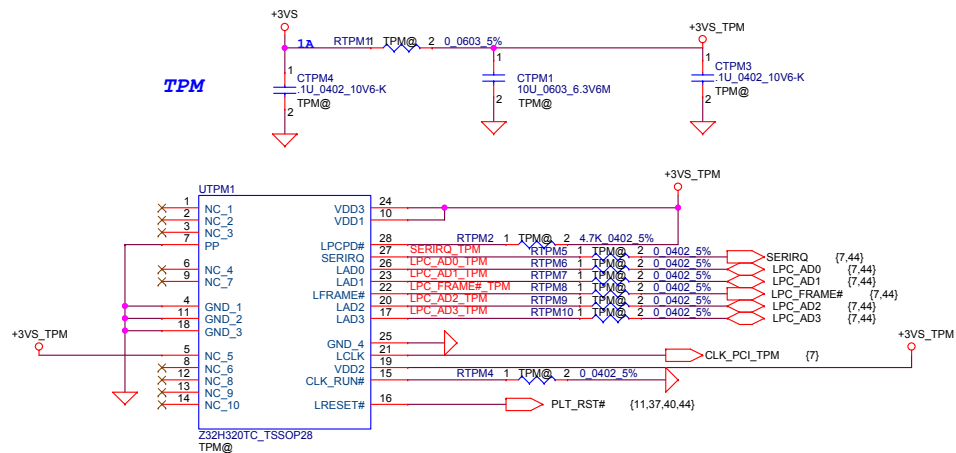



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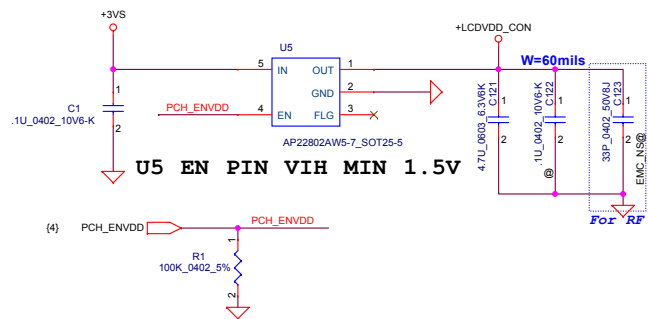
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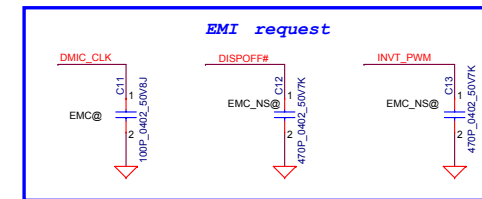
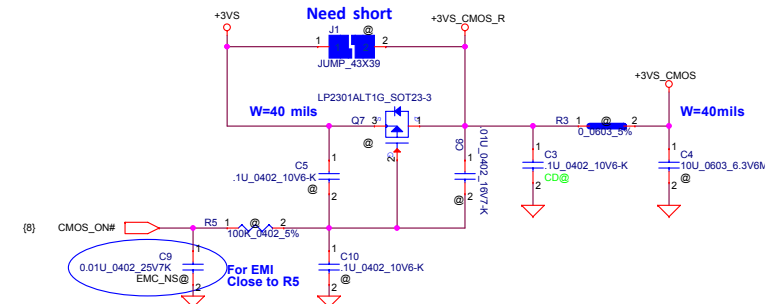


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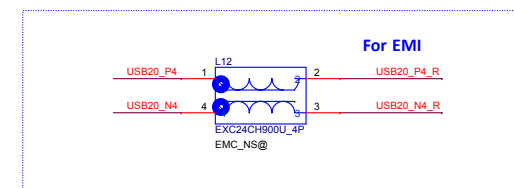
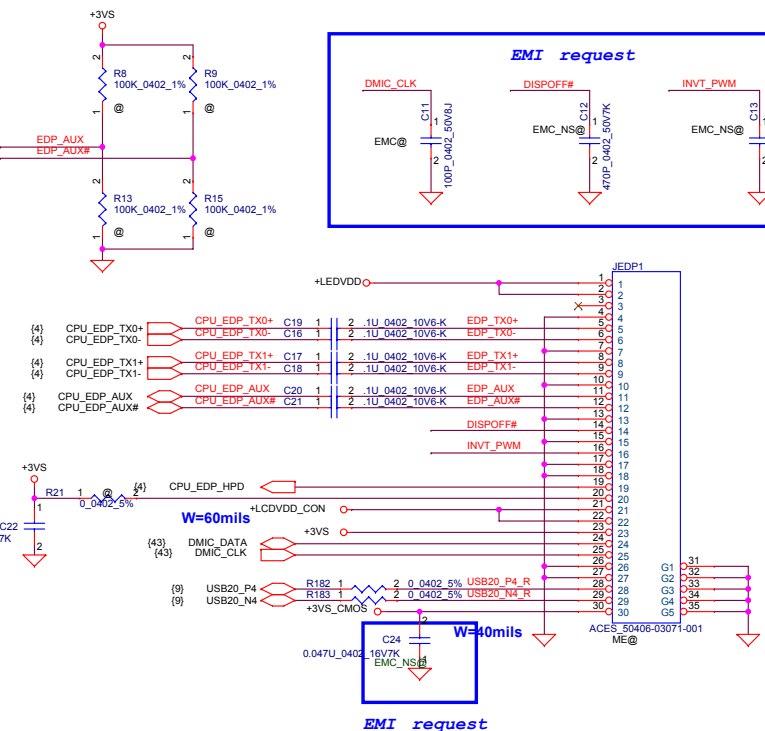
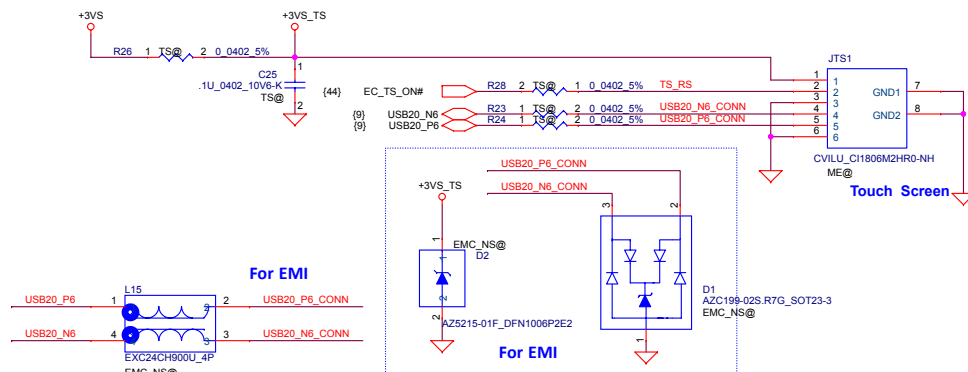
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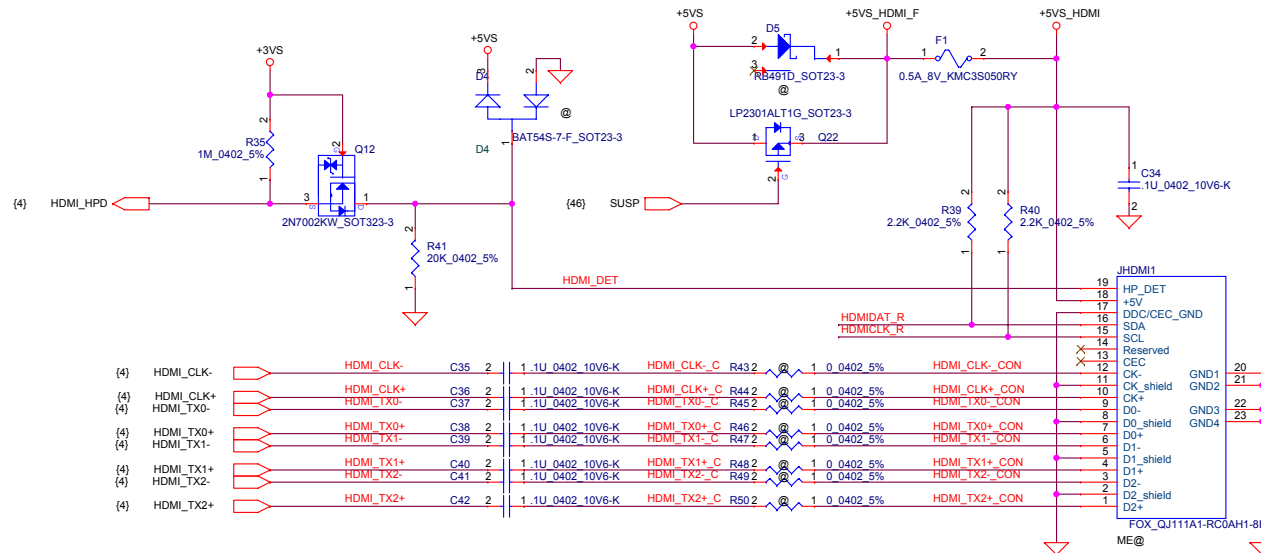
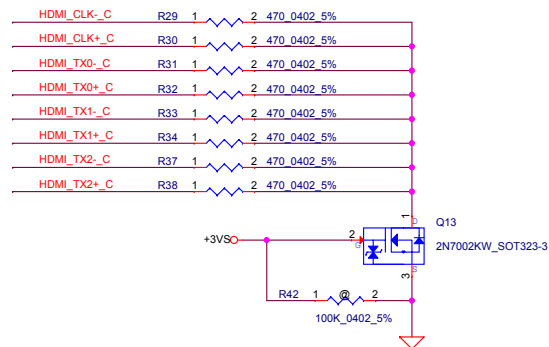
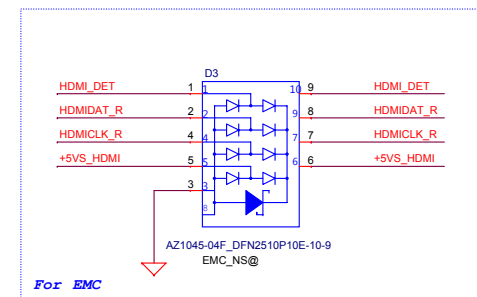
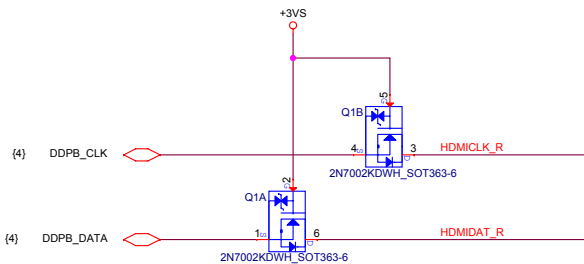
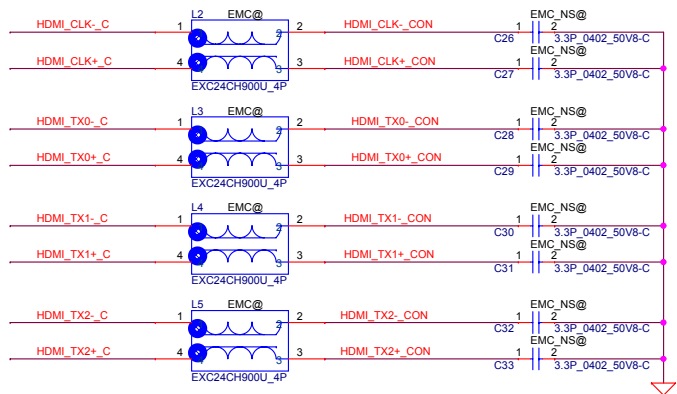


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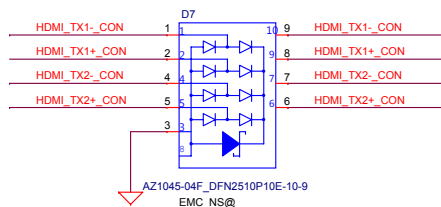
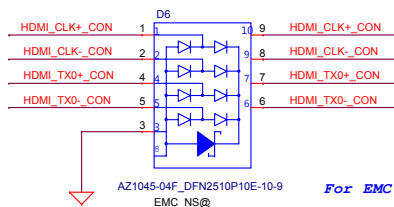



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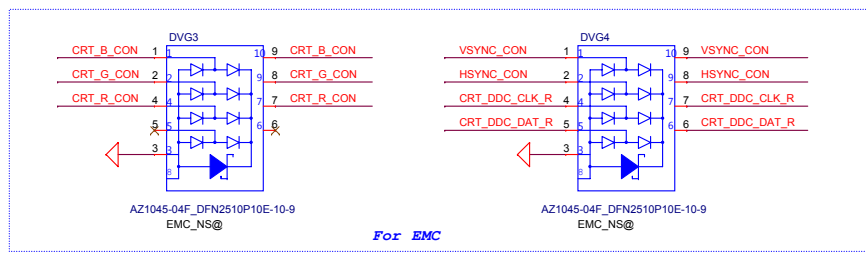
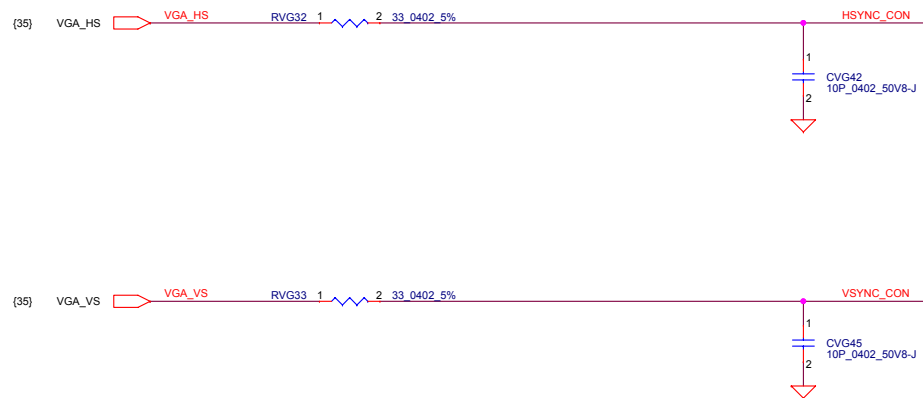
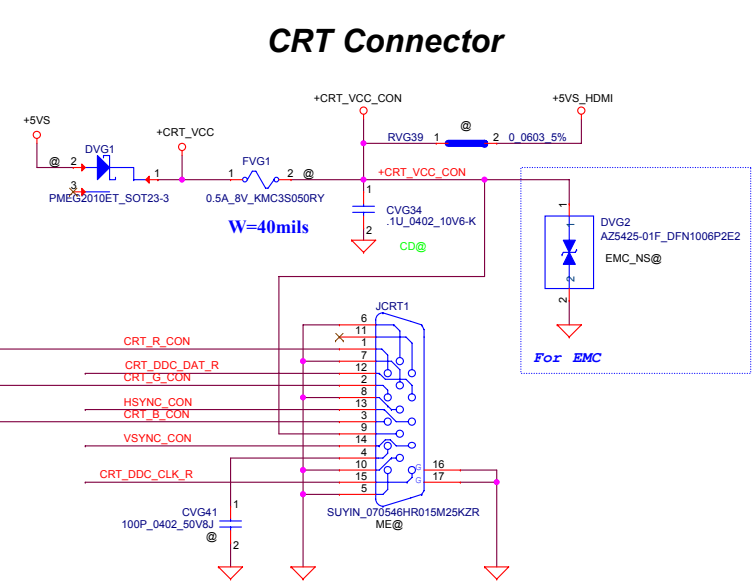
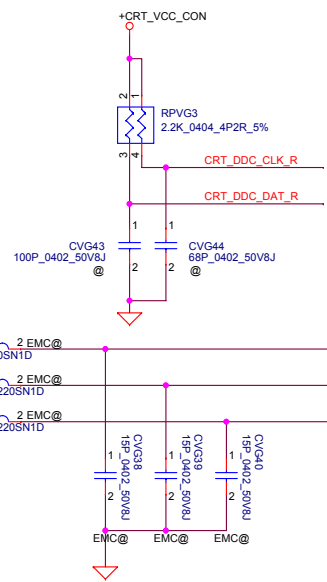
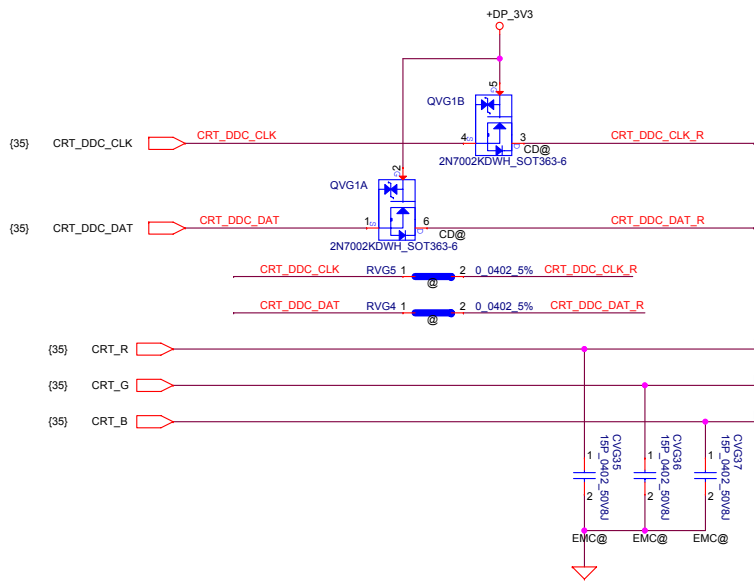




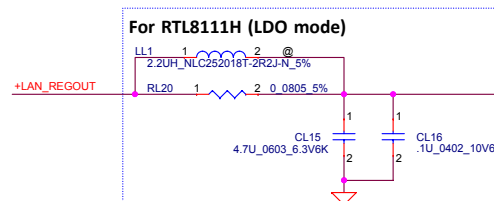
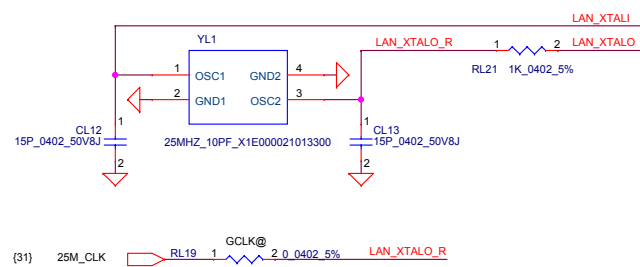
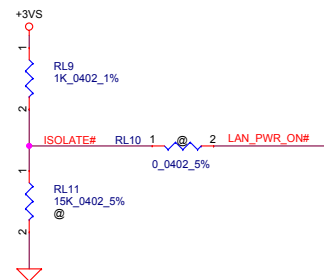
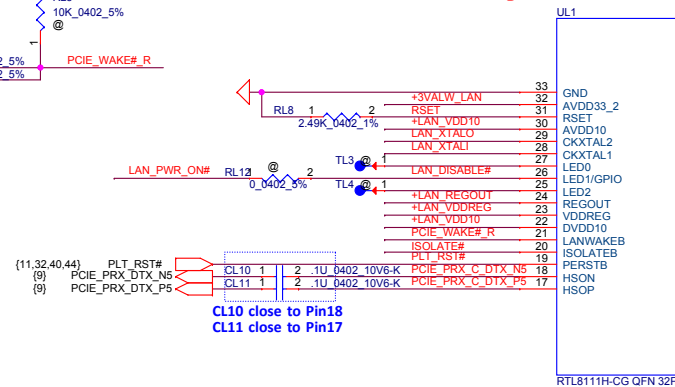
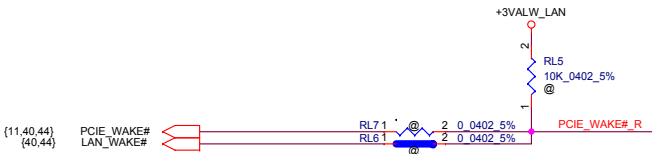
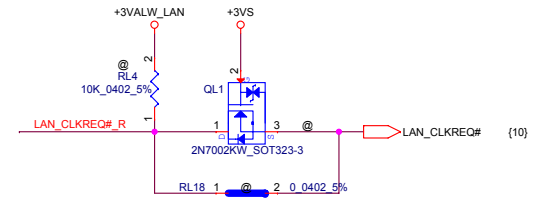
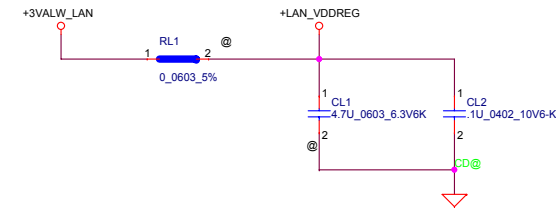
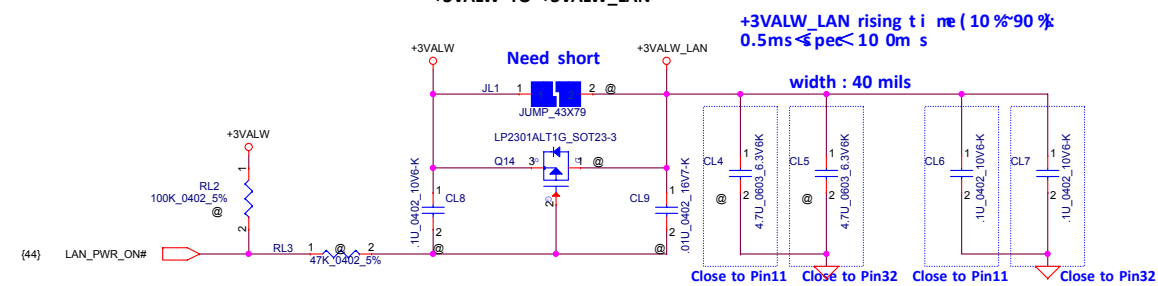
Close to JHDMI1



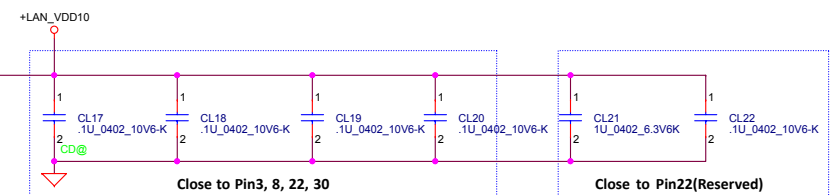
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2014/12/11	Deciphered Date	2015/12/11	HDMI_CONN		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number	Rev
				Custom	BMWQ1&2_UMA	0.2
				Date:	Monday, July 27, 2015	Sheet 34 of 60




CRT Connector

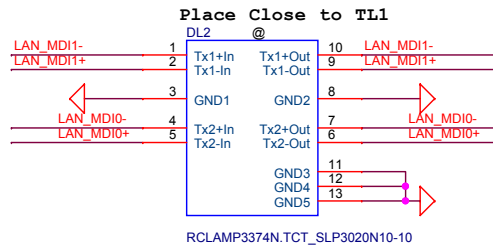
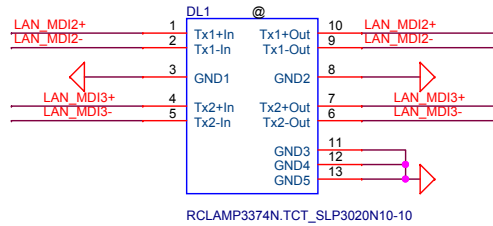


Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

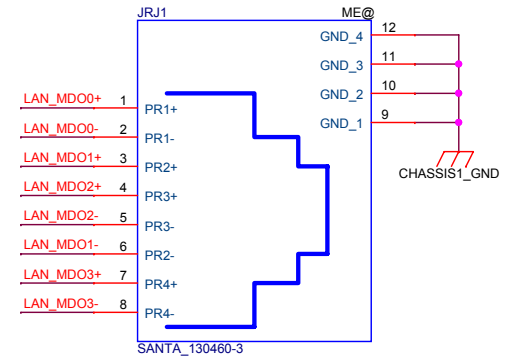
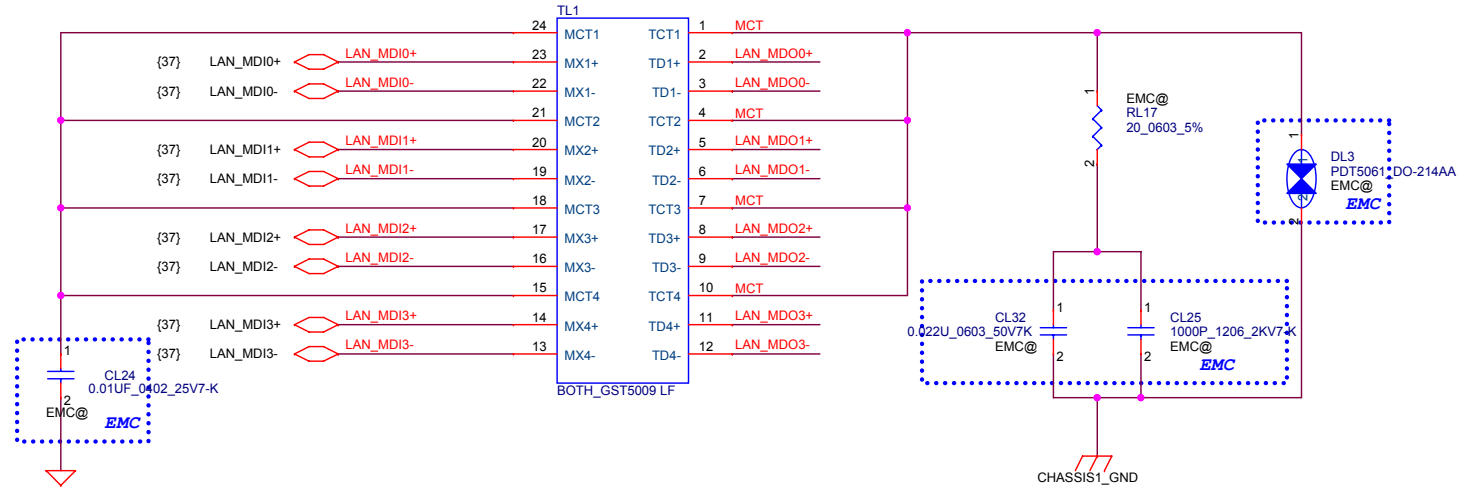
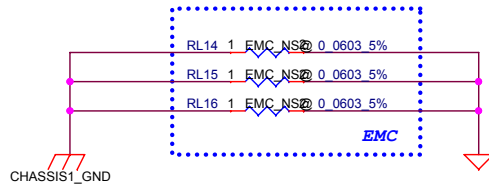


Security Classification		LC Future Center Secret Data		Title			
Issued Date	2014/12/11	Deciphered Date	2015/12/11	LAN_RTL8111H_CG			
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DL1/DL2
1'S PN:SC400007R00

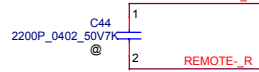


Place Close to TL2



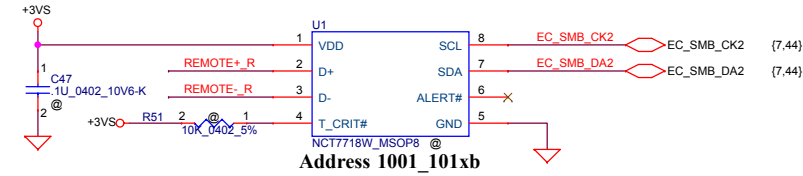
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/12/11	Deciphered Date	2015/12/11	LAN_Transformer	
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				Date:	Monday, July 27, 2015
				Sheet	38 of 60

Close to U1

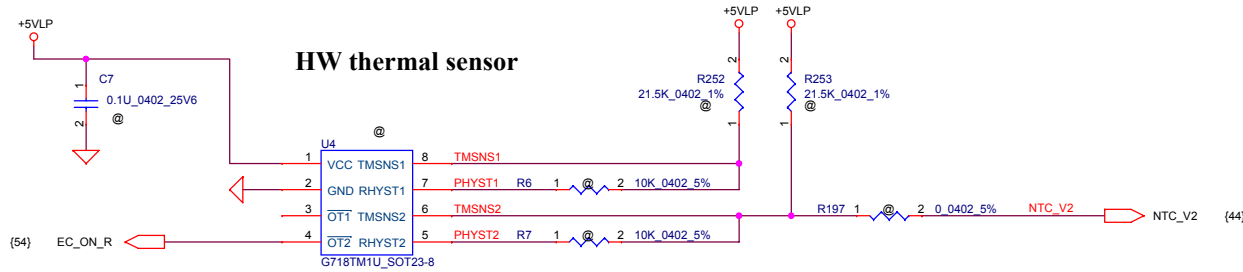


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

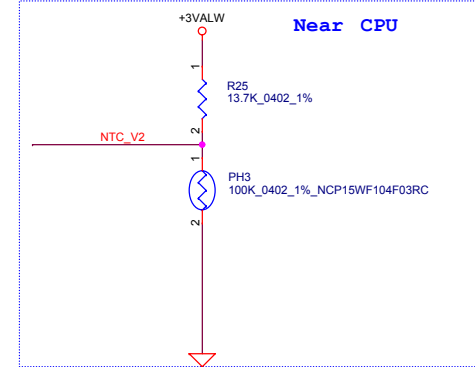
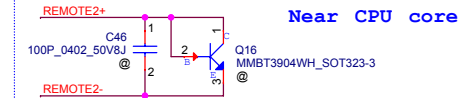
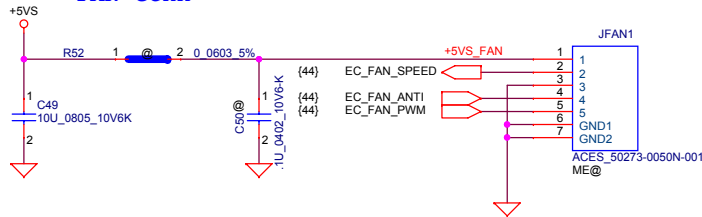


HW thermal sensor



over temperature threshold:
 $RSET = 3 * RTMH$
92+/-30C
Hysteresis temperature threshold.
 $RHYST = (RSET * RTML) / (3 * RTML - RSET)$
56+/-30C

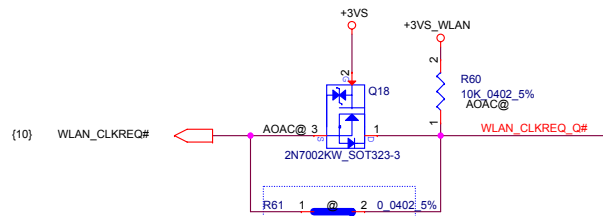
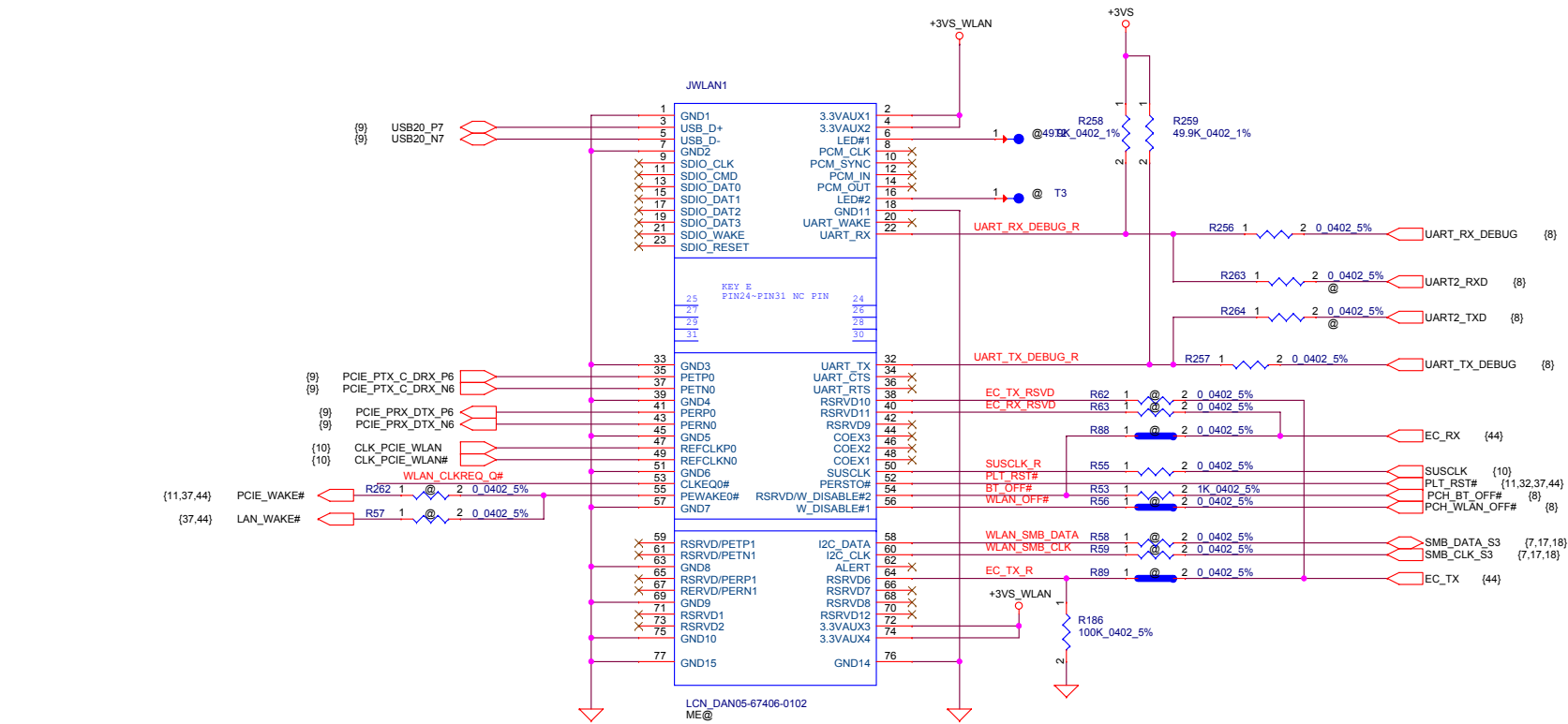
FAN Conn



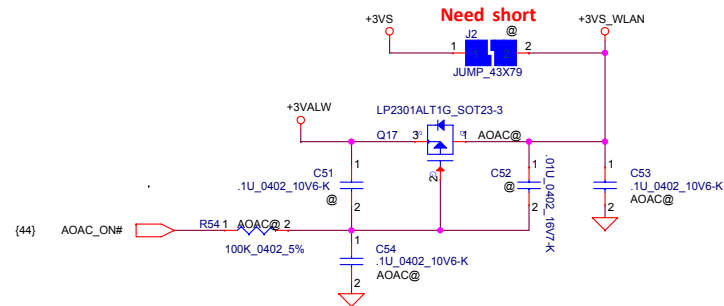
for layout optimized, change the EC_AGND to GND

Security Classification	LC Future Center Secret Data			Title
Issued Date	2014/12/11	Deciphered Date	2015/12/11	Thermal sensor/FAN CONN/TPM
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				Document Number
				Rev 0.2
				Date: Monday, July 27, 2015
				Sheet 39 of 60


Mini-Express Card(WLAN/WiMAX)



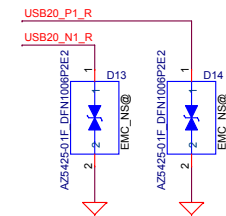
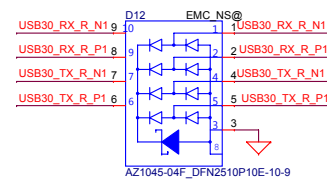
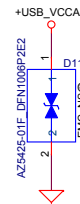
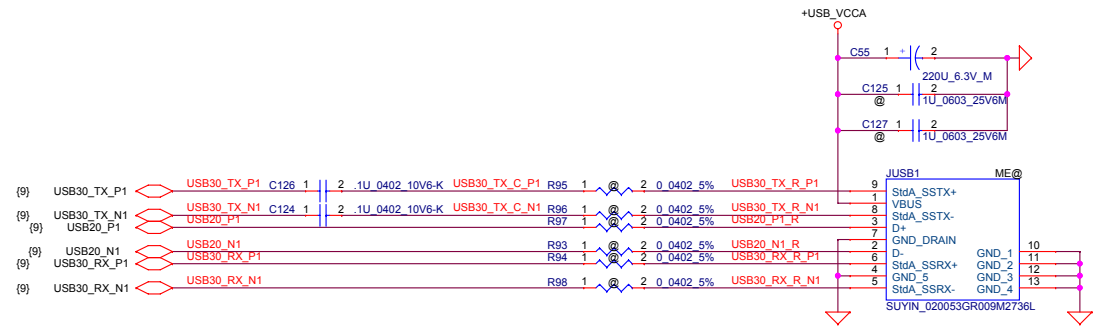
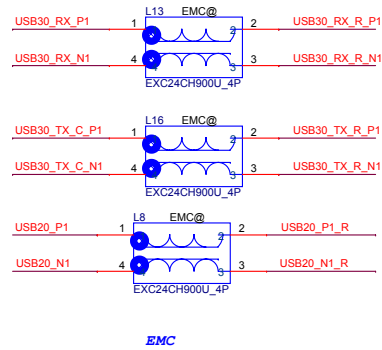
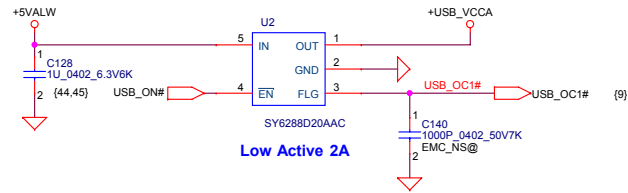
If support AOAC, NC R61;
if not support AOAC, stuff R61.




Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/12/11	Deciphered Date	2015/12/11	NGFF WLAN	
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				Custom	
				BMWQ1&2 UMA	
Date: Monday, July 27, 2015				Sheet 40 of 60	

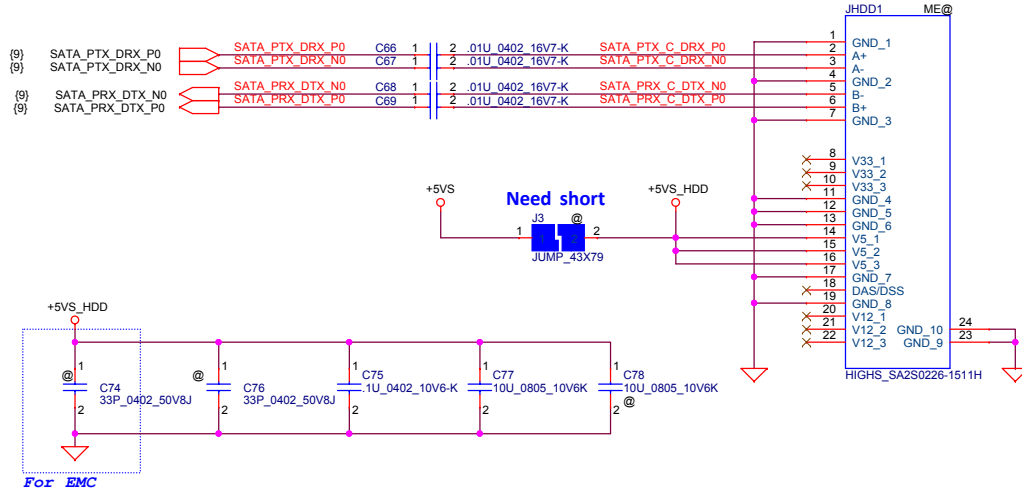


LEFT SIDE USB3.0 PORT x1

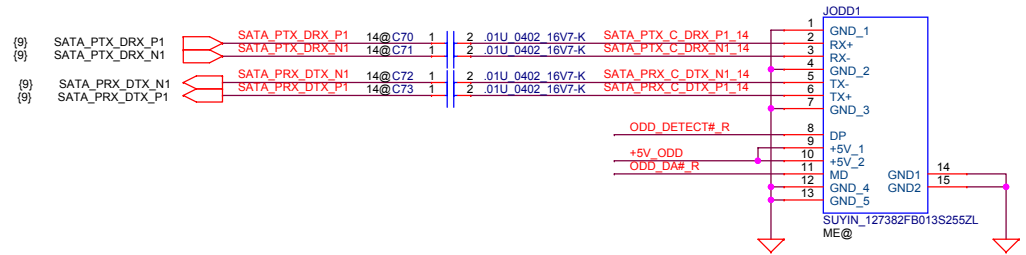


Security Classification		LC Future Center Secret Data				Title					
Issued Date		2014/12/11		Deciphered Date		2015/12/11					
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						Size		Document Number		Rev	
						Custom		BMWQ162 UMA		0.2	
Date:						Monday, July 27, 2015		Sheet 41 of 60			

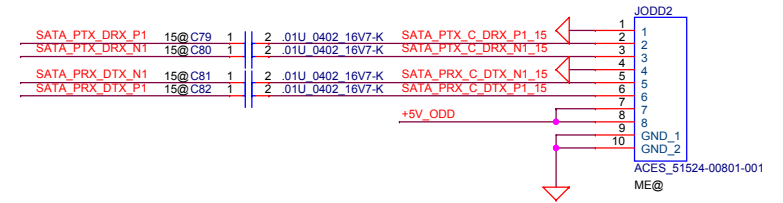
SATA HDD Conn.



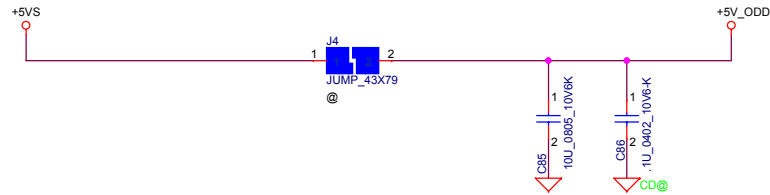
FOR 14" SATA ODD Conn.




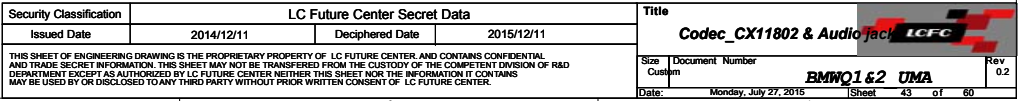
FOR 15" SATA ODD FFC Conn



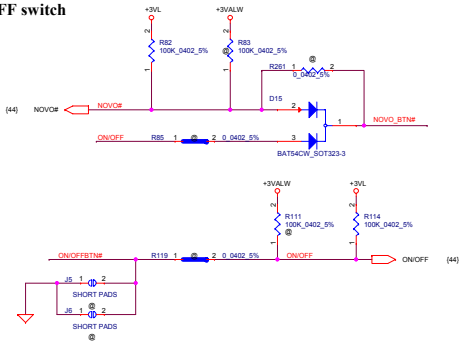
Need Short



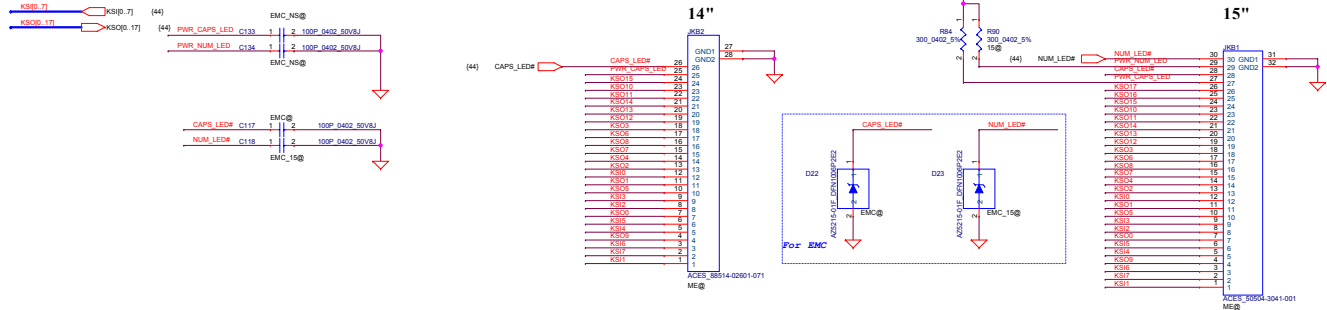
Security Classification		LC Future Center Secret Data				Title									
Issued Date		2014/12/11		Deciphered Date		2015/12/11				HDD/ODD CONN					
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Date:		Monday, July 27, 2015				Sheet		42		of		60			



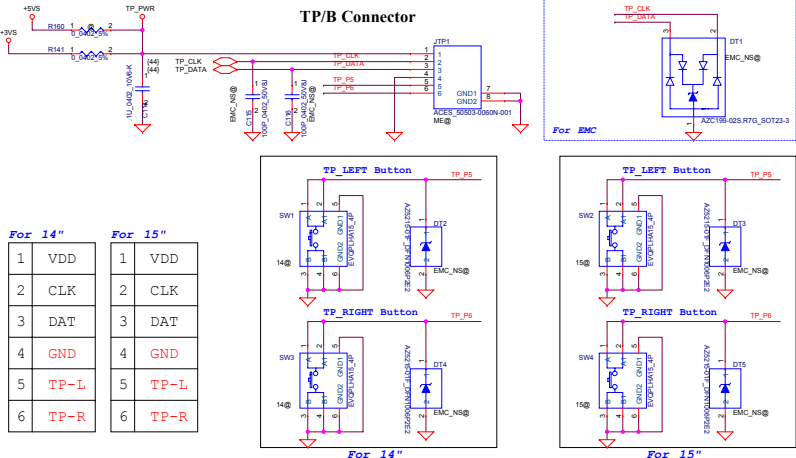
ON/OFF switch



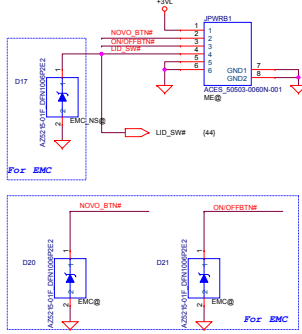
K/B Connector



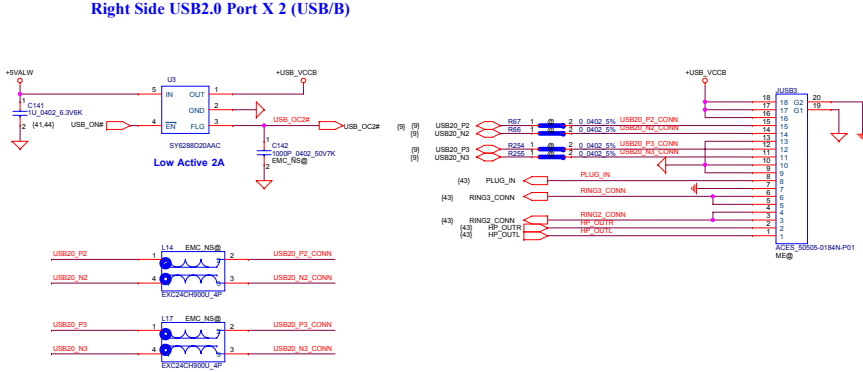
TP/B Connector



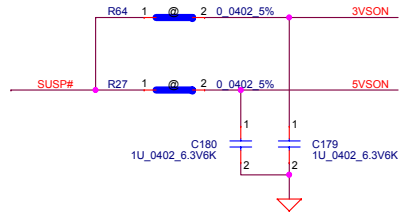
PWR/B Connector



USB I/O Connector



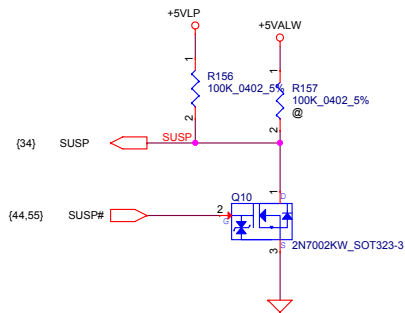
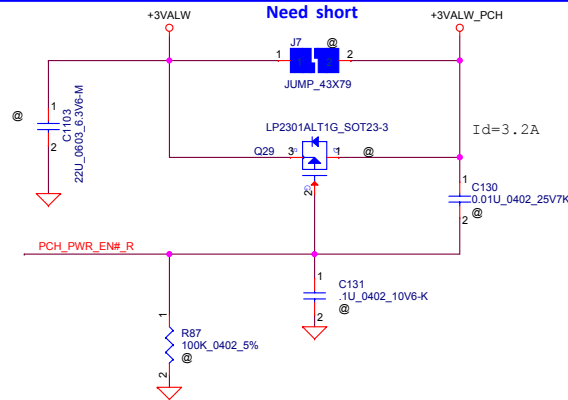
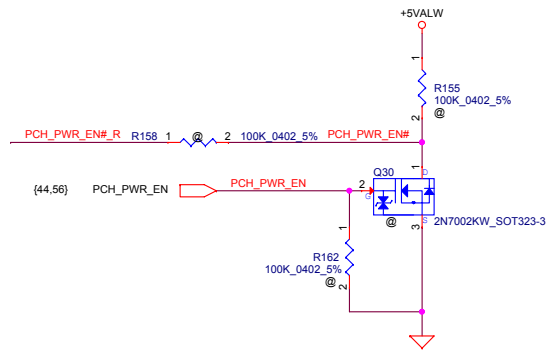
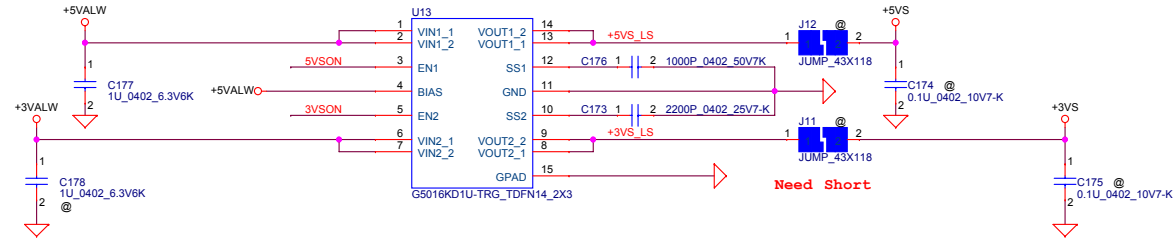
For 14"	For 15"
1 VDD	1 VDD
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 GND
5 TP-L	5 TP-L
6 TP-R	6 TP-R



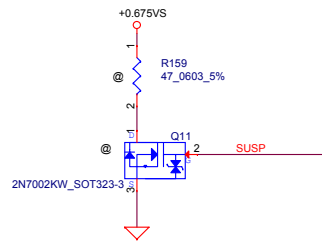
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

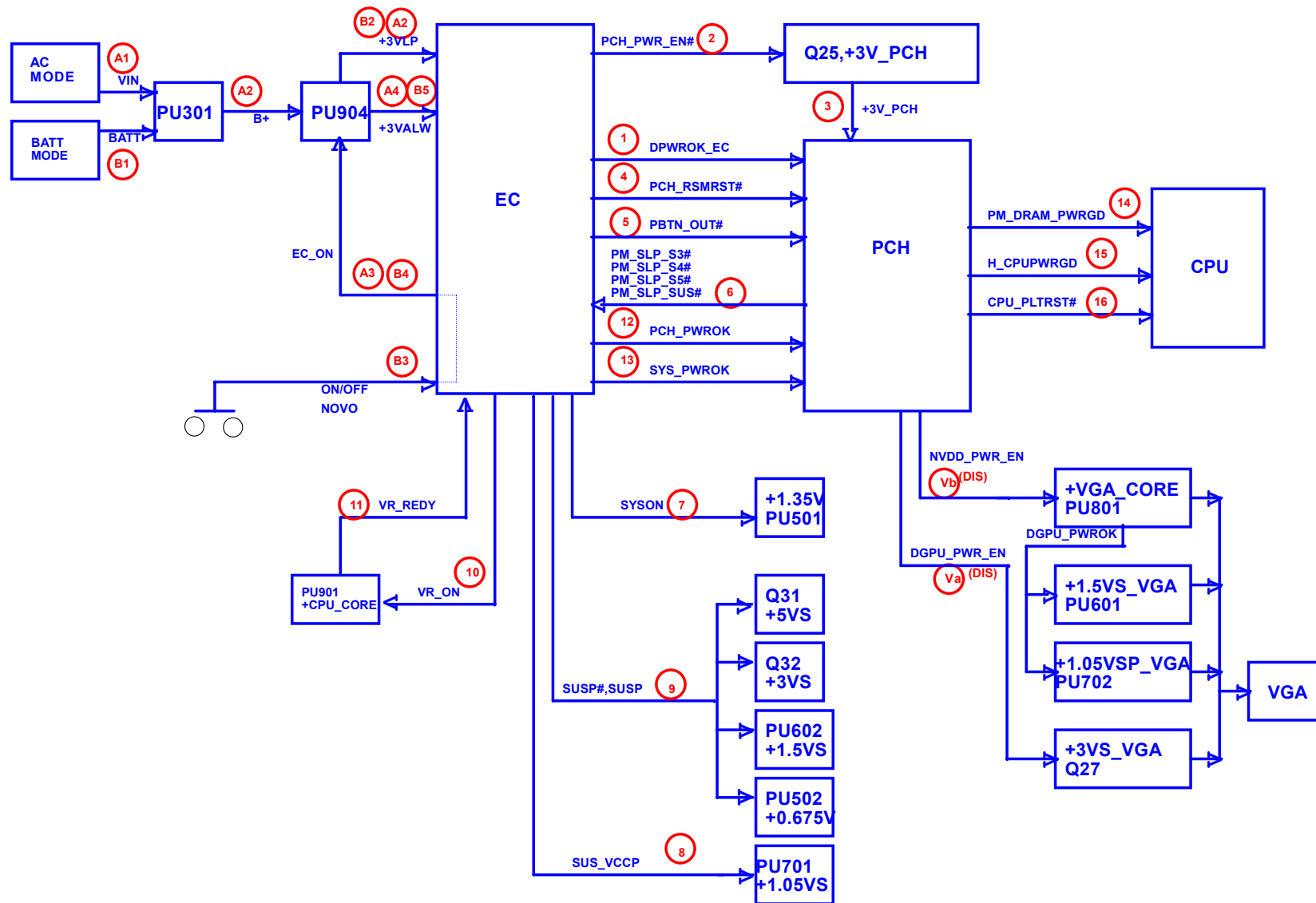
VIN 5V and 3.3V (VBias=5V), I_{MAX(per channel)}=6A, R_{ds}=16mohm



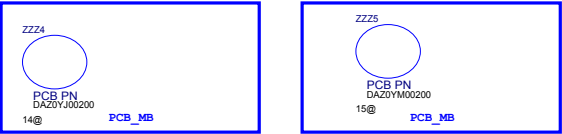
For DisCharge



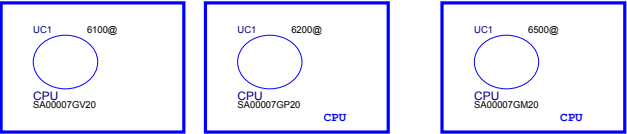
Security Classification				LC Future Center Secret Data				Title	
Issued Date				2014/12/11		Deciphered Date		2015/12/11	
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				Custom		BMWQ1&2 UMA		0.2	
				Date:		Monday, July 27, 2015		Sheet 46 of 60	



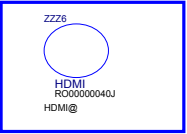
PCB



CPU

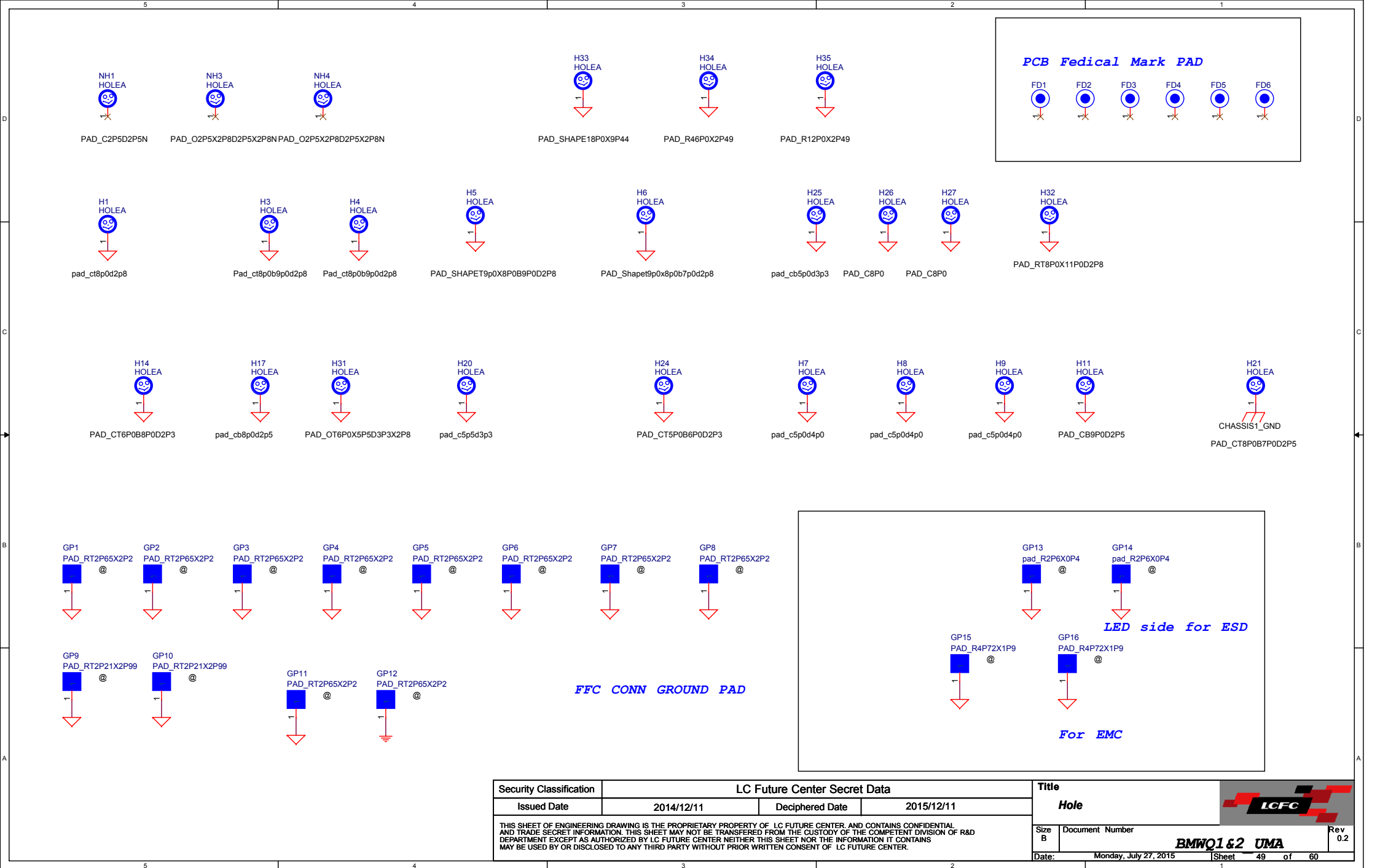



HDMI

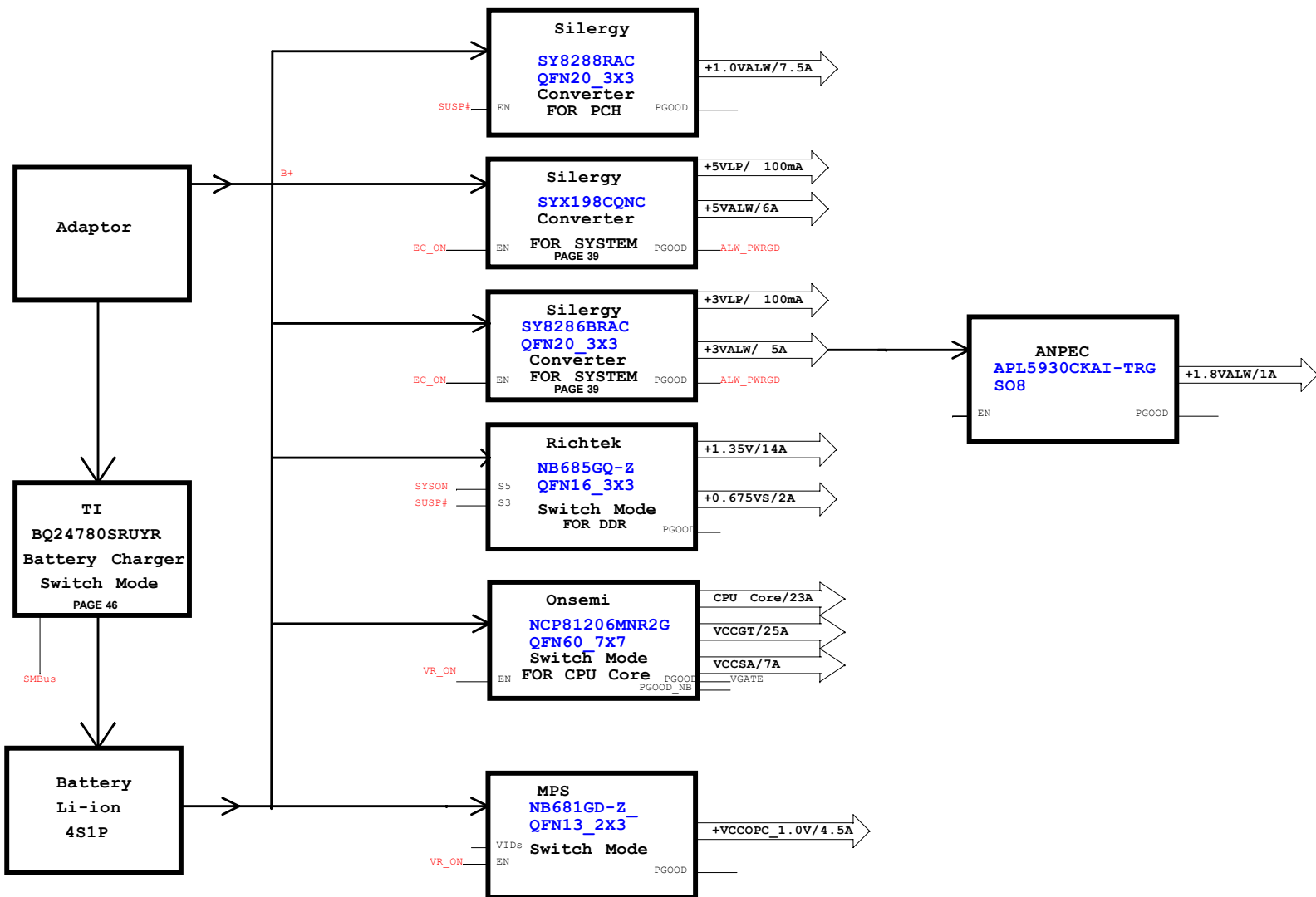


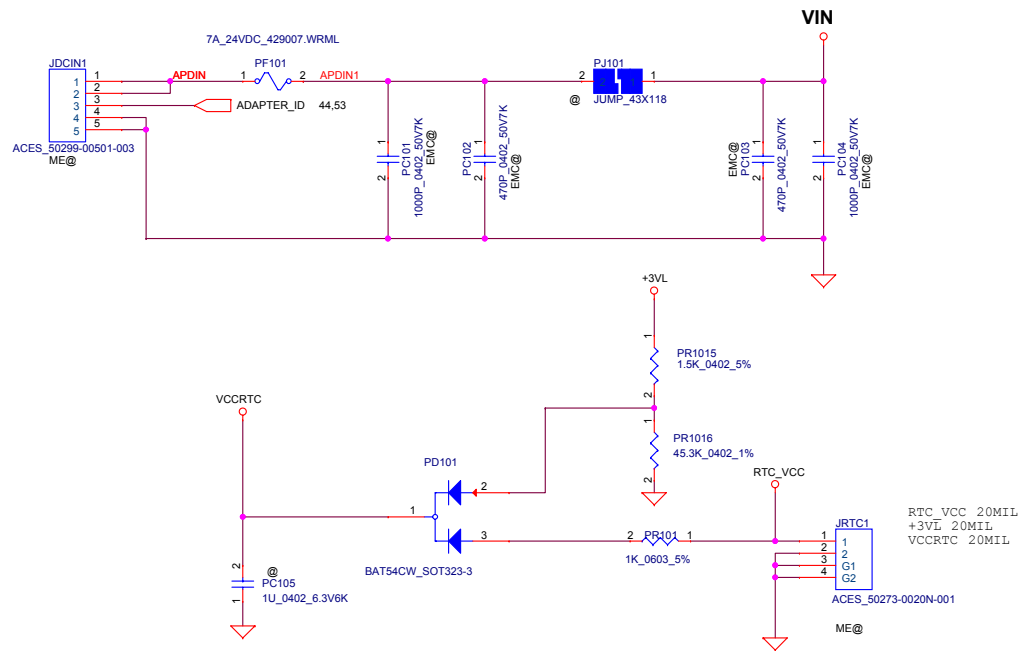
Board ID


BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	1	14" + Jet-LE + Single-Rank sku	RC107,RC108,RC109,RC121
0	0	1	1	14" + Jet-LE + Dual-Rank sku	RC107,RC108,RC102,RC121
0	1	0	1	15" + Jet-LE + Single-Rank sku	RC107,RC101,RC109,RC121
0	1	1	1	15" + Jet-LE + Dual-Rank sku	RC107,RC101,RC102,RC121
1	0	0	1	14" + Topaz-XT + Single-Rank sku	RC108,RC108,RC109,RC121
1	0	1	1	14" + Topaz-XT + Dual-Rank sku	RC108,RC108,RC102,RC121
1	1	0	1	15" + Topaz-XT + Single-Rank sku	RC108,RC101,RC109,RC121
1	1	1	1	15" + Topaz-XT + Dual-Rank sku	RC108,RC101,RC102,RC121

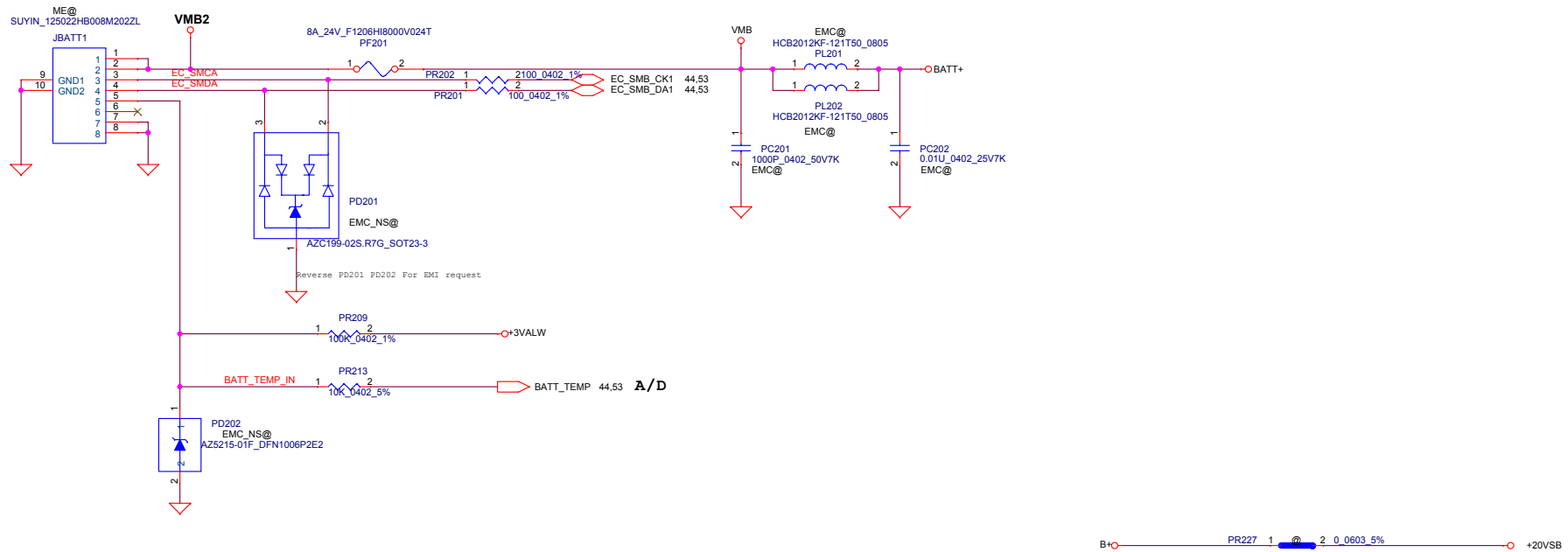


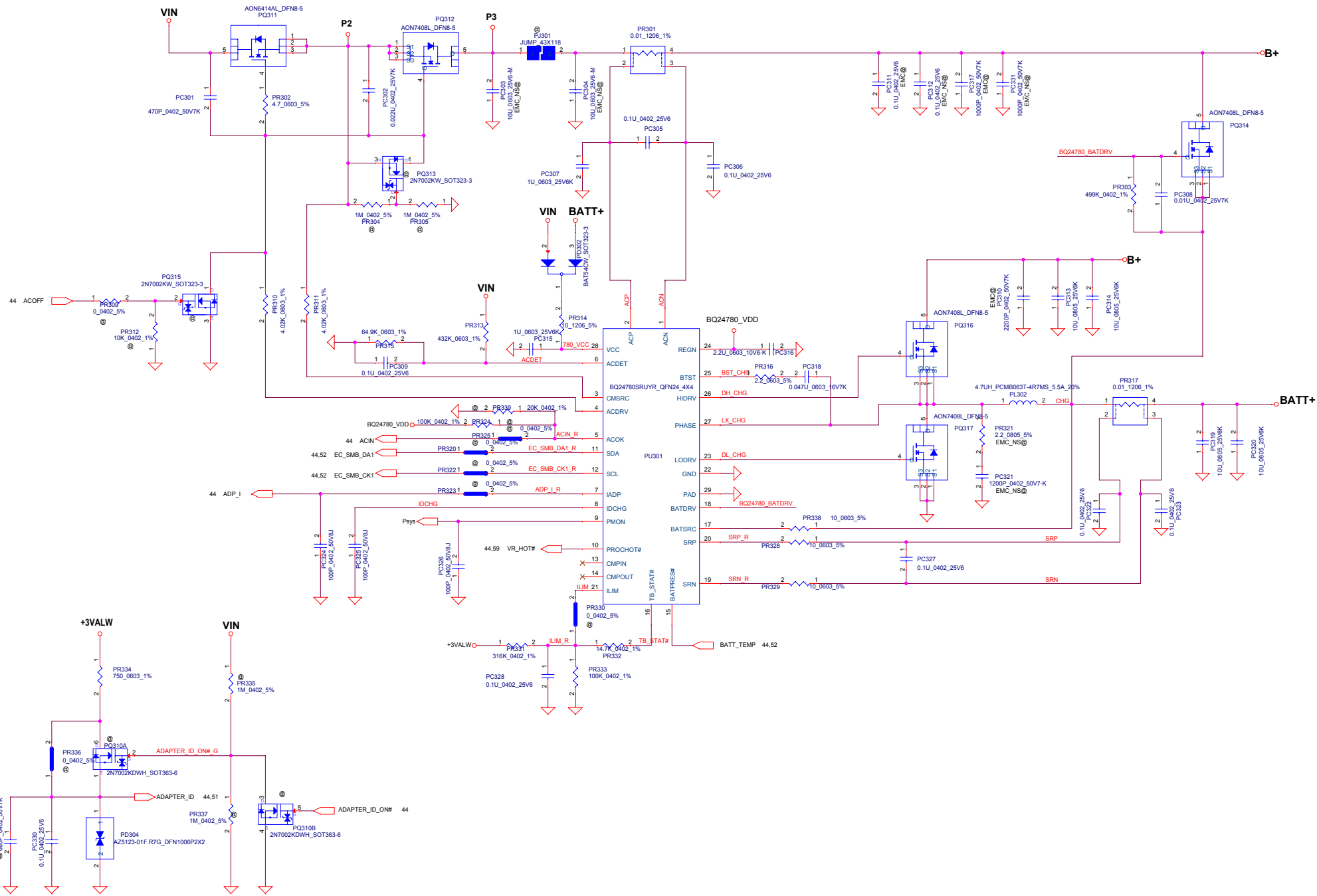
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2014/12/11	Deciphered Date	2015/12/11	Hole		
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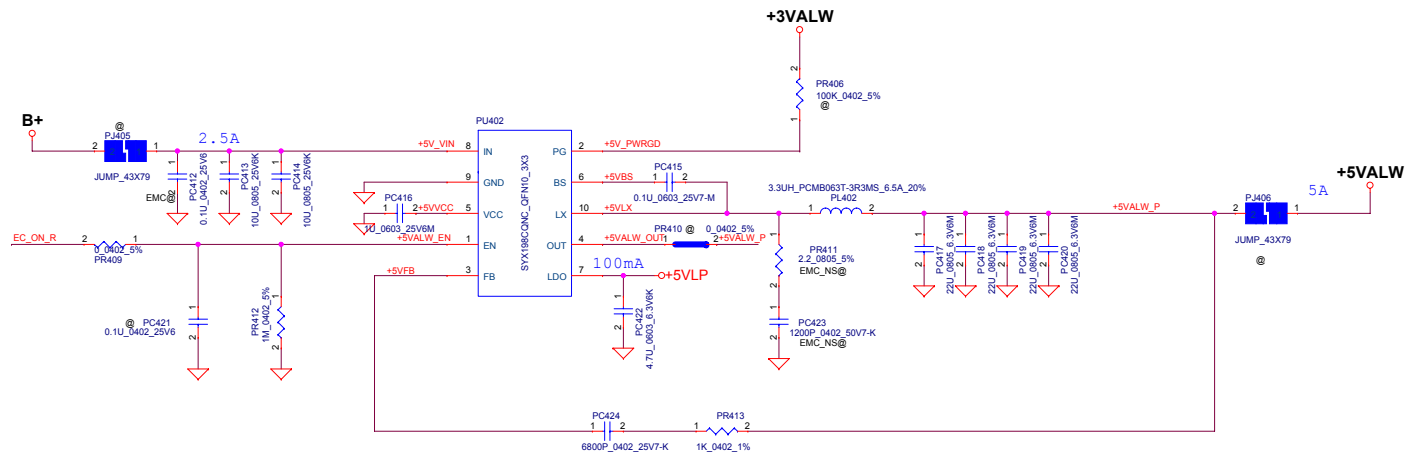
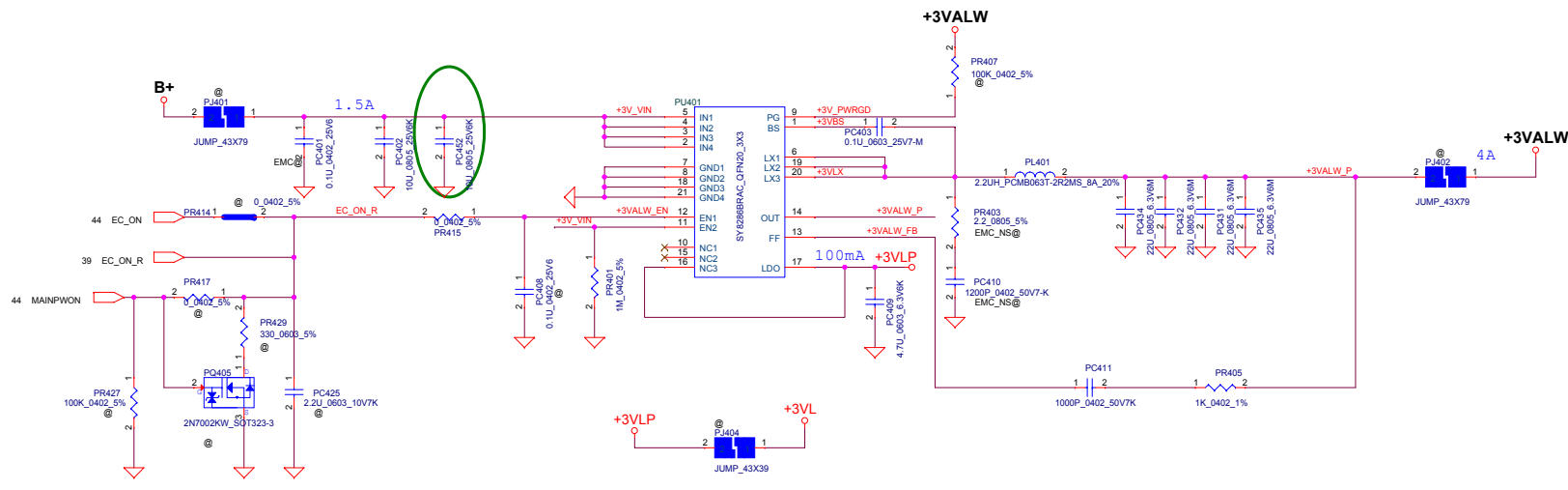




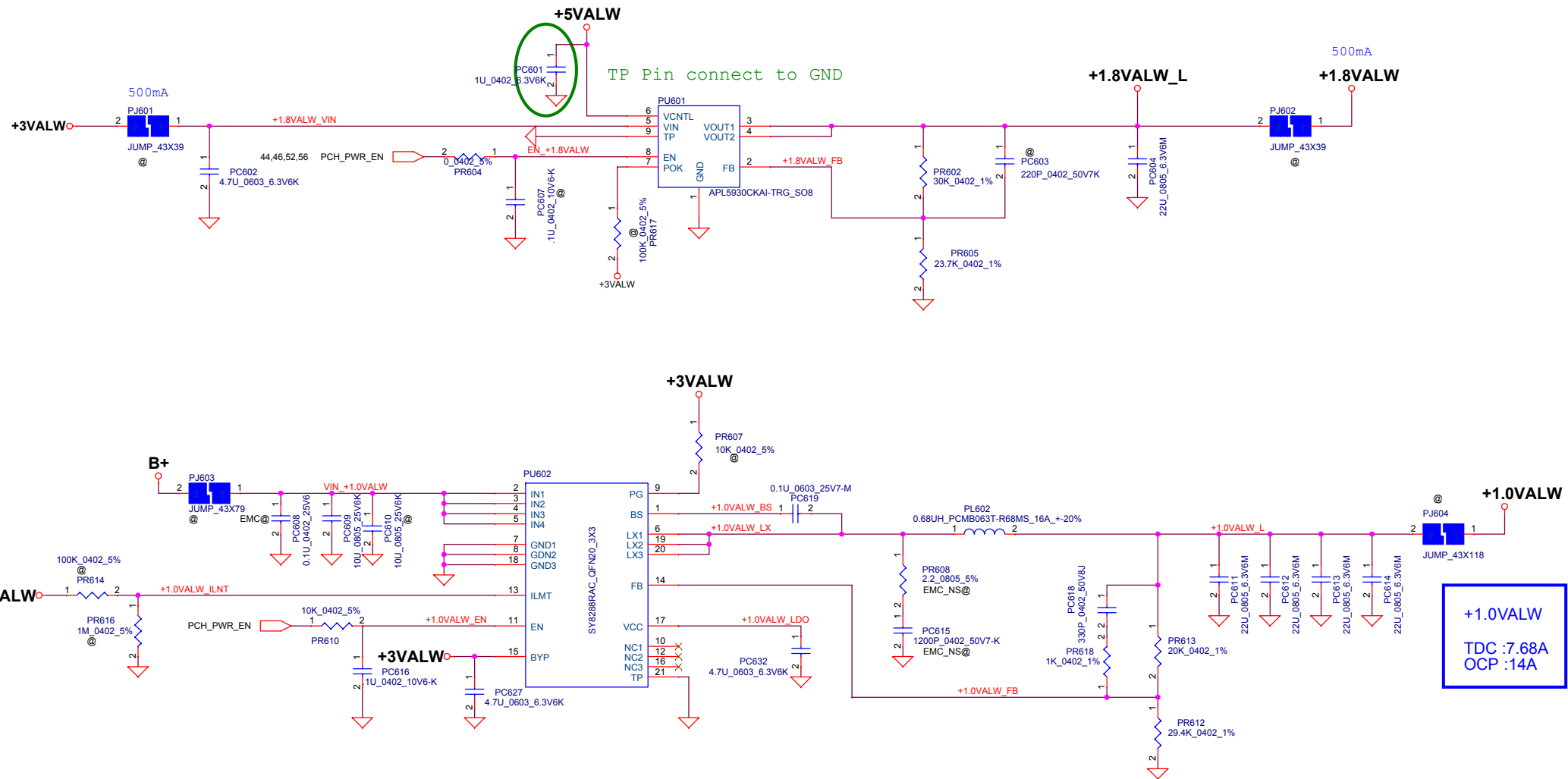
Security Classification		LC Future Center Secret Data				Title			
Issued Date		2013/08/08		Deciphered Date		2013/08/05			DCIN / RTC
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						Custom		BMQ1&Q2	0.1
						Date:	Monday, July 27, 2015	Sheet	51 of 60








6800pf soft start 2ms
47nF soft start 7ms



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title			
+1.8VAWL/+1.0VALW			
Size	Document Number	Rev	
Custom	BMQ1&Q2	0.1	
Date:	Monday, July 27, 2015	Sheet	56 of 60

